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# DESIGN AND DEVELOPMENT OF AN HF ANTENNA SYSTEM TUNER

A STUDY COMMISSIONED
BY
COMMUNICATIONS RESEARCH CENTRE

DSS CONTRACT 36001-0-3595/01-ST

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# DESIGN AND DEVELOPMENT OF AN HF ANTENNA SYSTEM TUNER

## SUMMARY

This report describes the design and development of an automatic HF tuner done under a research and development contract with the Communications Research Centre. The HF tuner was designed to match into an efficient antenna developed at CRC to improve the performance of short range sky-wave communications. The HF tuner which feeds a balanced antenna system is unique. It uses solid state PIN diode switches capable of handling 1000 watts of transmitter power to select the tuning components in a matching π-network. Circuits are incorporated into the tuner system to measures the antenna impedance. From a knowledge of the antenna impedance a microprocessor computes the initial components values required in a matching π-network. The final component values are selected using an fine tuning algorithm that quickly provides a low value of VSWR. Measurements indicate the tuner can switch within less than a millisecond to any frequency in the band from 2 to 15 MHz. Much development work was done on the PIN diode switches and the π-network configuration. Sufficient funds were not granted to finalize the design of the digital controller, construct the measurement circuit boards or integrate the various systems into an operating tuner.

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Contract 36001-0-3595/01-ST

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| T-11005/1-5 | Digital Controller |
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# DESIGN AND DEVELOPMENT OF AN HF ANTENNA SYSTEM TUNER

Contract 36001-0-3595/01-ST

## 1.0 INTRODUCTION

HF sky-wave communications over short distances is employed in both military and civilian operations. In order to improve the performance of HF communications over these short ranges, the Communications Research Centre developed a 3-wire dipole antenna fed by a balanced transmission line. This type of antenna radiates the energy efficiently at high angles of elevation over the frequency range from 2 to 15 MHz. A balanced antenna tuner installed at the base of the tower is required to match the unbalanced 50 ohm output impedance of the transmitter to the input impedance of the balanced transmission line for maximum transfer of RF transmitter power. If the operating frequency is continuously altered in order to avoid jamming in a hostile environment, the antenna tuner must be quickly tuned at a new operating frequency. Automatic antenna tuners using mechanical relays have been built and tested but their lifetime is severely limited if the operating frequency is altered many times per second at high transmitter powers. Some tuners using all solid state components have been developed for radio amateur usage but their transmitter power rating is limited to about 30 to 50 watts for continuous transmissions over a period of about 10 minutes. At the date this report was written, there is still not a reliable automatic antenna tuner with a balanced output feed capable of handling 1 kWatt of transmitter power and continuously switching to any frequency in the HF band within several milliseconds.

In late February 1991, the Communications Research Centre awarded Petrie Telecommunications Ltd a research and development contract (DSS 36001-0-3595/01-ST) to design and develop an HF antenna tuner for military operations. In July 1992, we informed all parties concerned with the contact that 70% of the allocated funds had been expended and additional funds were required to complete the contract. In the winter of 1992/93, approval was obtained to use the remaining contract funds to develop a PC operated controller. In early 1993, we were informed additional funds were not available to complete the project and all research and development work ended on March 31, 1993. In the fall of 1993, additional funds were assigned to generate this report which describes the work undertaken in the design and development of the HF antenna tuner.

Petrie Telecommunications Ltd staff were responsible for the overall direction of the research and development work. T. Daniels from Daniels Electronics Ltd provided advice and consulting services in the initial stages of the contract on the overall development of the tuner. J. Strickland of Diversitel Communications was subcontracted to design and develop a controller and to provide advice on the matching network. R. Bonnycastle of Electronic Engineering Ltd was subcontracted to assist on the

design of the antenna measurement circuits and to decrease the switching time of the PIN diode circuits. Routes Inc was subcontracted to design and supply a controller and a PC operated microprocessor that would process the data from the measurement circuits and provide suitable signals to drive the PIN diode switches. The name, address and telephone numbers of the main person responsible for the subcontracted work are provided in Appendix A.

This report describes the design and the development of an HF tuner performed under DSS Contract 36001-0-3595/01-ST. A general description of the HF tuner and its operation is presented in Section 2. The four major systems that form the tuner are described in the following sections of the report. The RF measurement system provides parameters that enable the signal frequency and the antenna impedance to be computed by a microprocessor. The proposed operation and design of the RF measurement system including circuit diagrams are presented in Section 3. A detailed description of a proposed matching network is presented in Section 4. The design of the PIN diode switcher unit is presented in Section 5 with measurements of the isolation and switching times for an initial circuit design. A final circuit is described capable of switching the PIN diode drivers in a shorter period. In Section 6, information is presented on the initial circuit design for the controller that was built and tested. Section 7 describes detailed computations to be performed by the microprocessor for selecting the initial inductors and capacitors in the matching network as well as computations to quickly adjust the network after the initial components are selected. In Section 8, estimates are given of the maximum length of time the tuner takes to match a transmitter to the CRC antenna system. The work completed under this contract and the work still required to complete the tuner are summarized in Section 9. The conclusions of this report are presented in Section 10.

## 2.0 DESCRIPTION OF ANTENNA TUNER

The antenna tuner is designed to meet the following main specifications indicated in the research and development contract;

| | |
|---|---|
| Operating Frequency Range: | 2 to 15 MHz |
| RF Power Rating: | 1 kWatt PEP continuous |
| Type of Switching: | Solid State |
| VSWR: | ≤ 2.0:1 |
| Tuning Time: | ≤ 25 ms |
| Operating Temperature: | -40°C to +40°C |
| Max. Period of Transmission: | 20 minutes |

The block diagram of the proposed antenna tuner is shown in Fig. 1 with the transmitter and antenna system on opposite ends of the tuner. The tuner is designed to match a 1 kWatt continuous duty transmitter with a 50 ohm RF output impedance to a balanced transmission line that feeds a 3-wire dipole antenna developed by CRC. The tuner's transmitter input consists of a balun that provides a 50 ohm unbalanced to 100 ohm balanced feed to the antenna system. When the transmitter power is initially applied to the antenna tuner, an attenuator pad with a nominal 50 ohm input/output impedance is connected across the balun and antenna without any matching network. The RF measurement system provides parameters to determine the forward and reflected voltages, the phase difference between these voltages as well as the operating frequency. The measured values are fed to a microprocessor by a controller. The microprocessor computes the antenna impedance and the initial values of inductance and capacitances for the matching network. The controller then selects these initial values of components in the network.

After the initial values of the components are selected for the matching network, measurements of the forward and reflected voltages are repeated. These measurements are fed to the microprocessor and a fine tuning adjustment is made to the inductances and capacitances in the matching network. The microprocessor is programmed to allow up to a maximum of ten fine tuning steps. When either the VSWR is less than 1.6:1 or the maximum number of fine tuning steps is attained the attenuator is disconnected. For matching the impedances of the CRC antenna, the VSWR will be less than 2.0:1 at all operating frequencies in the frequency range from 2 to 15 MHz. The tuner is designed to complete this matching operation in less than a few millisecs.

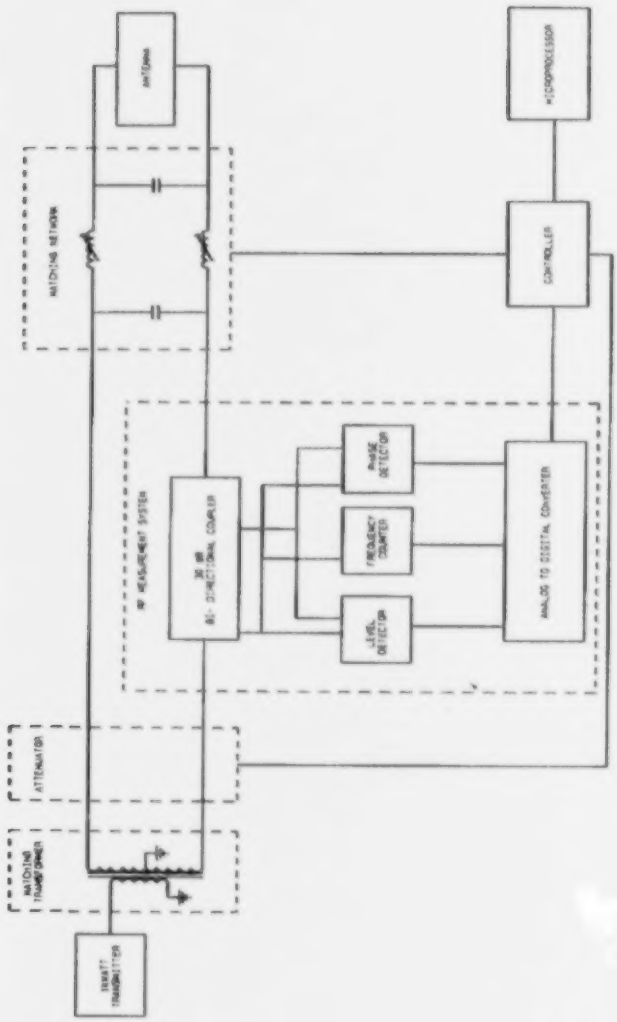


Fig. 1 BLOCK DIAGRAM OF HF TUNER

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## 3.0 RF MEASUREMENT SYSTEM

The RF measurement system uses the outputs of a bi-directional coupler to provide parameters that enable the computation of the signal frequency, the VSWR, and the complex impedance of the input terminals to the antenna system. A block diagram of the RF measurement system is shown in Fig. 2. The system consists of a bi-directional coupler, several measurement circuits and signal conditioning circuits that are described in detail in the following sections.

### 3.1 Bi-directional Coupler

In Fig. 2, the bi-directional coupler couples the forward and reflected signals to two output ports based on the direction of the signal flow. The specifications are as follows for an Anzac CH-130-4 bi-directional coupler proposed for the tuner:

| | |
|---|---|
| Power Rating | 500 watts |
| Frequency Range | 2-32 MHz |
| Coupling (Input to Output) | 30 ±0.5 dB |
| Coupling Flatness | ±0.25 dB |
| VSWR (All ports) | 1.1:1 Max |
| Directivity (2-15 MHz) | 30 dB Min |
| Main Line Loss | 0.1 dB Max |

From measurements of the forward ($V_{FWD}$) and reflected ($V_{REF}$) voltages from the coupler and the phase difference ($\phi$) between these voltages, the complex antenna impedance ($Z=R+jX$) as well as the VSWR can be computed as follows:

$$Z = 50 \frac{1 - \Gamma (\cos\Theta + j\sin\Theta)}{1 + \Gamma (\cos\Theta + j\sin\Theta)}$$

$$VSWR = \left| \frac{1 - \Gamma (\cos\Theta + j\sin\Theta)}{1 + \Gamma (\cos\Theta + j\sin\Theta)} \right|$$

where $\Gamma = V_{REF}/V_{FWD}$

$\Theta$ = Phase difference between $V_{FWD}$ and $V_{REF}$

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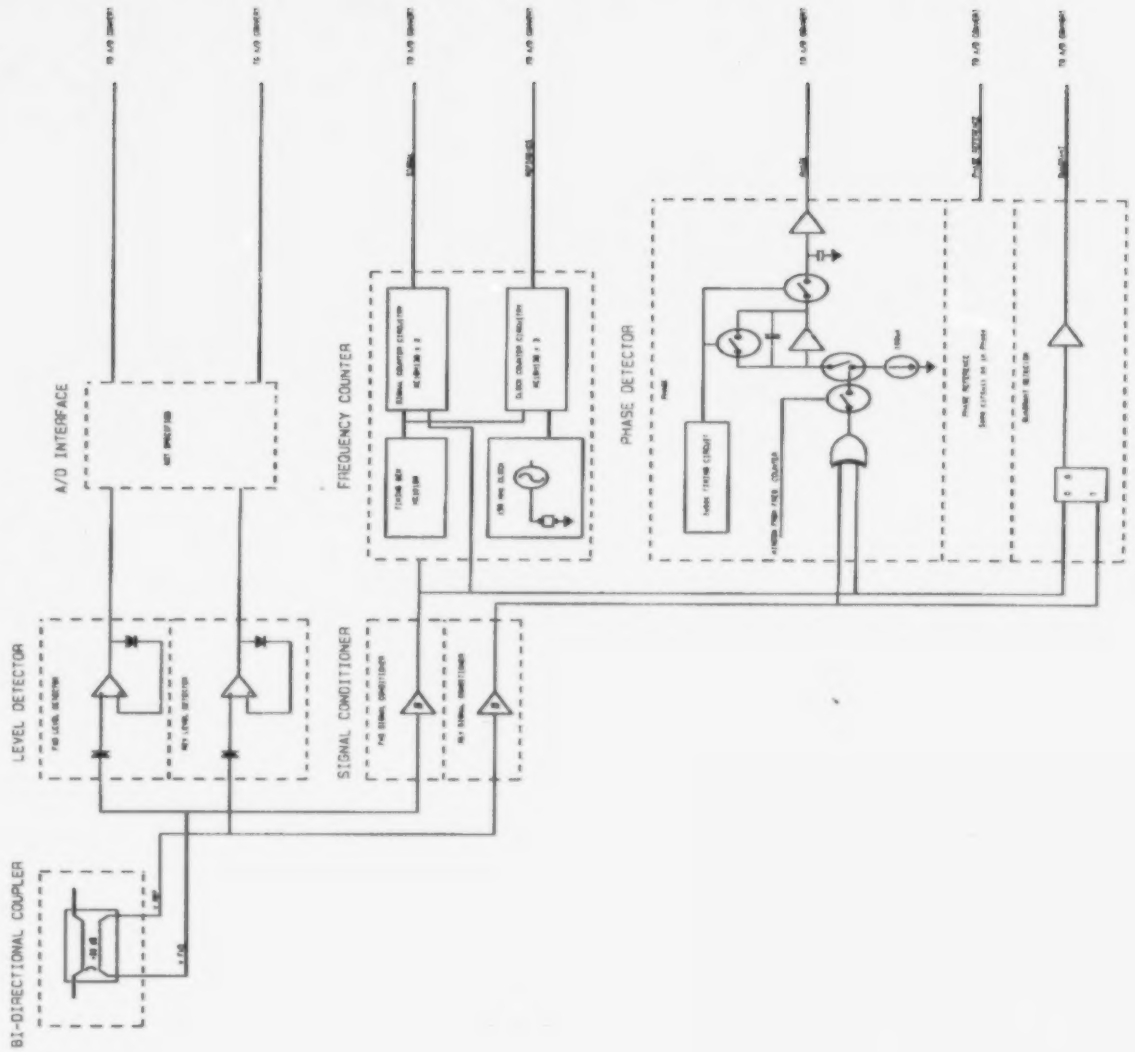


Fig. 2 BLOCK DIAGRAM OF RF MEASUREMENT SYSTEM

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### 3.2 Level Detector

The forward and reflected voltage levels of the RF signals from the bi-directional coupler are measured by the level detector circuit shown in Diagram T-11000. This circuit is similar to that developed by Grebenkemper[2]. It consists, of a matched pair of Schottky diodes, a filter and an operational amplifier with low offset voltages and leakage currents. The signal is rectified by diodes D1 and is filtered by C1, C2, C3 and R1 and R2. The non-linearity in the detecting diode D1 is compensated by U1 and a feedback diode D2. The diodes D1 and D2 are selected to have similar current conducting characteristics.

The level detector provides a logarithmic output proportional to the RF input voltage and is linear over an 80 dB dynamic range. Measurements of its linearity are shown in Fig. 3 for a frequency of about 15 MHz. Similar measurements of the linearity were obtained for a frequency of 2 MHz.

### 3.3 Signal Conditioner

The conditioning circuit in Fig. 2 converts the sine wave of both the $V_{FWD}$ and $V_{REF}$ signals from the bi-directional coupler to square wave signals. These latter signals are then used by the digital circuitry to measure the signal frequency and the phase difference between $V_{FWD}$ and $V_{REF}$. A high speed comparator from Analog Devices with ECL output levels generates the square wave. A dual package comparator is used to minimize any phase shift between $V_{FWD}$ and $V_{REF}$ created by propagation delays in the electronic circuitry.

The detailed circuit diagram of the signal conditioner is shown in Diagram T-11000. The device U2 compares the analog signal from the directional coupler to a ground reference connected to its inverting input. When the analog voltage on the noninverting input is greater than the reference voltage, the Q output will be high and its complimentary output will be low. The outputs of U2 are squared again by U3 an ECL triple line receiver. All ECL outputs are terminated with 50Ω to a -2.0V reference level and unused inputs connected to VBB. Q1 and its associated circuitry provides the -2.0V reference level from a -5.2V power supply required by the ECL devices.

### 3.4 Frequency Counter

The frequency counter shown in Fig. 2 provides an output representing both the signal and reference frequency. The circuit operates by generating a nominal 10 usec window which contains the exact integer number of cycles corresponding to the frequency of the input signal. The number of cycles of a 150 MHz reference signal (fc) is also counted over the duration of this nominal 10 usec window. The frequency of the RF input signal is given by

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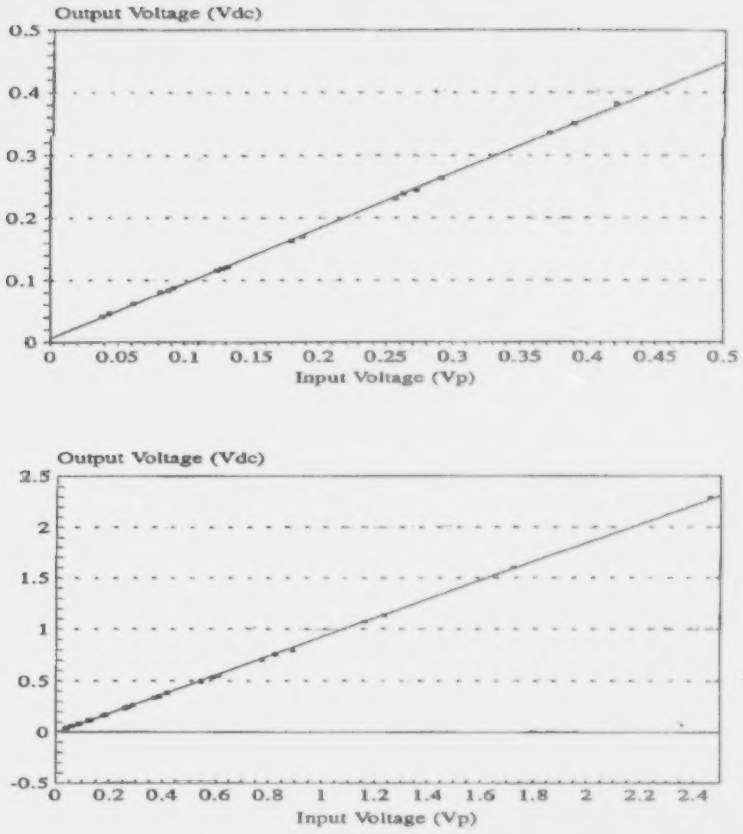


Fig. 3 LINEARITY OF DETECTOR CIRCUIT

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$$fs = fc\ [Ns/Nc]$$

where fc = frequency of reference signal
Ns = number of signal cycles in window
Nc = number of cycles of the 150 MHz signal in window

The accuracy of the measured frequency is defined by the accuracy of the reference frequency and the resolution determined by ± 1 count in the number of cycles of the 150 MHz reference signal. For a 150 MHz reference signal and a nominal 10 usec window the resolution is 1 part in 1500 or 667 ppm.

A detailed schematic of the frequency circuit is shown in Diagrams T-11001. The circuit timing is controlled by three signals namely a data request signal from the micro-processor, a 10 usec window created by U3 and the count window generated at U4 in T-11001/1. The data request signal from the micro-processor is first converted to an ECL logic level by U2 (TTL to MCEL translator) and its associated circuitry. The output of U2 then initiates a 10 usec window and presets all counter (U6 to U10) to a logic 0. The 10 usec window is triggered by the input signal fs at U4. At the output of U4, the resulting "count window" consists of an integer number of cycles of fs. Two counter U6 and U7 then count the number of signal cycles (Ns) during the period of the count window. Three more counters U8,U9 and U10 count the number of cycles of the 150 MHz reference signal (Nc) during the count window period. A crystal oscillator is used to generates the 150 MHz reference signal. U5 determines when the counter is idle and thus indicates that the data is valid. Once U5 has determined that the data is valid, all counter outputs are latched to their corresponding MCEL to TTL translators (U16 to U20) via AND gates U11 to U15 in T-11001/2&3. The data valid signal and the counter outputs are then buffered and fed to the micro-processor.

### 3.5 Phase Detector

The phase detector consists of a phase circuit, a phase reference circuit and a quadrant detector circuit as shown in Fig. 2. As in the case of the frequency circuit, a nominal 10 usec window is generated which contains the exact integer number of cycles corresponding to the frequency of the input signal. For each cycle of the signal frequency, a pulse is generated whose width corresponds to the phase difference between the forward voltage $V_{FWD}$ and reflected voltage $V_{REF}$. These pulses are integrated over a period of N cycles of the signal frequency in the nominal 10 usec window. At the same time the phase of the signal is being measured, a phase reference voltage is generated by integrating a continuously generated signal over the nominal 10 usec window using an identical phase circuit. The quadrant detector circuit determines if $V_{FWD}$ leads or lags $V_{REF}$.

A detailed schematic of the phase circuit is shown in Diagram T-11002. A data request pulse generated by the microprocessor

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momentarily closes U5A in T-11002/1 that sets the initial output level to zero. Then an exclusive OR gate U1A generates a square wave whose width is proportional to the phase difference between $V_{FWD}$ and $V_{REF}$ signals. With U2 closed during the ≈10 usec window period, any "1" levels at the output of U1 will turn on Q1 and Q2 which allows a constant current of 100 uamps generated by Q3 and U3 to charge C1. After the ≈10 usec window closes switch U5B, a 1 usec pulse is generated by U6 and allows the integrated voltage level to be retained by a sample and hold circuitry U7 and U8. The circuitry for generating the phase reference voltage is identical to that for the signal voltage.

In the quadrant detector circuit, U12A in T-11002/2 determines if $V_{FWD}$ leads or lags $V_{REF}$ by generating either a high level "1" or "0" output. A high level "1" in the quadrant output detector represents an inductive load, while a low output "0" represents a capacitive load. In order to minimize false data, U12B only allows the output signal of U12A to be processed over the nominal 10 usec window.

### 3.6 Analog to Digital Converter

The analog to digital (A/D) converter is used as an interface between the measurement system and the controller. A block diagram of the A/D converter is shown in Fig. 4. The A/D converts both the analog and the parallel data signals from the measurement system to serial data. The serial data is then transmitted from the A/D converters to the controller via a fiber optics line.

A detailed schematic of the A/D converter circuit is shown in four diagrams labelled T-11003/1 to T-11003/4. In T-11003/4, Q2 receives the fiber optic RQST pulse. U23 regenerates the pulse as a 1.5 usec pulse. This STRB pulse is used to trigger the external phase and frequency measuring circuitry. The external circuitry issues ready flags (PHRDY and FREQRDY) when the respective data is valid. In the case of the phase measurement circuity, the data is in the form of two analog 0 to 2.5 volt signals corresponding to the phase between $V_{FWD}$ and $V_{REF}$ and the phase reference. The frequency measurement is in the form of two 12-bit (all 12 bits are not necessarily used) values, NS and NC. When both phase and frequency measurements are valid, U33B goes low. U29B synchronizes U33B with the 4 MHz ADCLK. U30, U31, U32 divides the 40 MHz clock by 10.

All four A/D converters (U3 and U6 in T-11003/1: U8 and U10 in T-11003/2) start their conversion simultaneously. The conversions take about 3 usec. Two of the four analog channels contain track and holds U2 and U5 in T-11003/1; Forward and Reverse voltages. The phase between $V_{FWD}$ and $V_{REF}$ and the phase reference channels do not need track-and-holds since they already employ track-and-holds in the phase measurement circuitry. Track and holds U2 and U5 hold their signals when the A/D conversions start. In addition, the quadrant bit QUAD is latched by U12A in T-11001/3.

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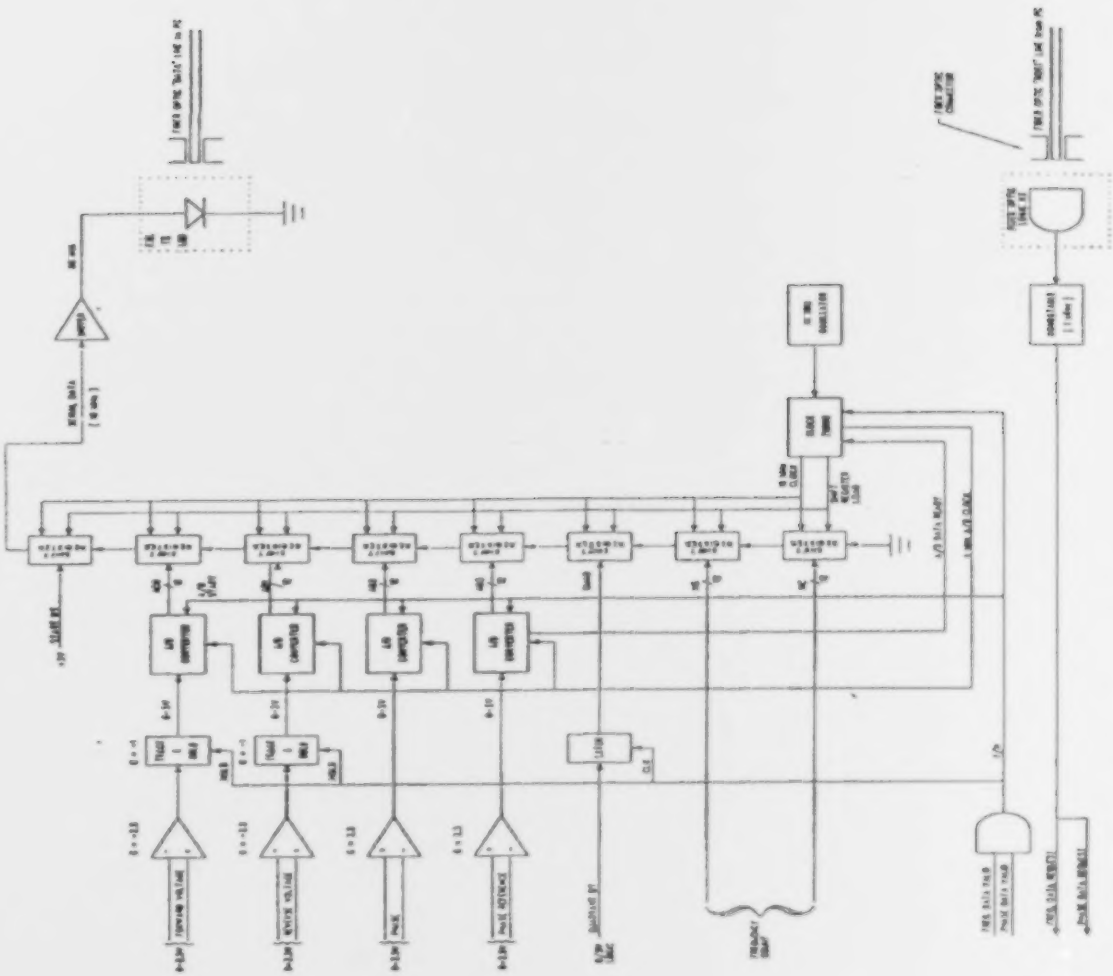

Fig. 4 BLOCK DIAGRAM OF ANALOG TO DIGITAL CONVERTER

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As the track-and-holds are inverting (G=-1), U1 and U4 shown in T-11003/1 invert the analog input signals. Amplifier U7 and U9 shown in T-11003/2 do not invert the signals. All amplifiers have a gain of 2 and an input resistance of about 2.2 K. Higher input resistances result in longer settling times; longer rise and fall times and underdamped pulse responses. All four input amplifiers are configured as differential inputs. The return is grounded at the driving end, avoiding low frequency ground loop currents in the grounds.

When the A/D conversions are complete, the /BUSY line goes high. The BUSY output of only one A/D is needed (U10 in T-11003/2). The three others will change state at the same time since all A/Ds are operated from the same ADCLK and the start convert (T/H) is synchronized with ADCLK. U27A and U27B shown in P11103/4 divide the 40 MHz clock by four to give the 10 MHz SRCLK signal. U28A synchronizes the /BUSY signal with the rising edges of SRCLK. When U28A goes high, U28B is set, causing /SRLD to go low, loading all the shift registers (U14A, U13, U15, U16 in T-11003/1; U17, U21, U22 in T-11003/2; U18, U19, U20, U24 in T-11003/3) with their respective data. One half clock cycle later, U28B is reset via U29A in T11003/4. U29A is then reset by U28B. U14A in T-11003/1 is set when the SRLD (shift register load) occurs, forming the start bit. Immediately after SRLD, the data is clocked-out at 10 MHz. U14B ensures that the start bit is synchronized with the 10 MHz clock and hence is exactly 100 nsec wide. In T-11003/1, Q1 drives the IR LED D1, at a current of about 80 mA.

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## 4.0 MATCHING NETWORK

### 4.1 General Description

The matching network enables maximum transfer of power between the 50 ohm output impedance of the transmitter and the impedance of the balanced transmission line feeding the antenna. The matching network is composed of capacitors, and inductors whose values are computed by the microprocessor and selected by the digital controller. It is proposed that a standard balanced π-network be utilized as the matching network. Depending on the impedances to be matched, the balanced π-network can be used in three possible configurations as shown in Fig. 5: two separate "L" network configurations or a combination of both "L" networks.

In an Report by Diversitel Communications[1], it was shown that the 50 ohm output impedance of a transmitter can be matched to the impedance of an antenna by choosing either an L-network or a π-network. It was concluded in the report that:

- antenna impedances whose real component exceeds 50 Ω can only be matched by a π-network,
- antenna impedances which lie within the circle of radius of 25 Ω centred at Ra = 25 Ω, Xa = 0 Ω on a Ra versus Xa plot can only be matched by an L-Network,
- antenna impedances which do not lie within the circle of radius 25 Ω centred at Ra = 25 Ω, Xa = 0 Ω, whose real component does not exceed 50 Ω, and whose imaginary component is positive can only be matched by a π-network,
- antenna impedances whose real component does not exceed 50 Ω and whose imaginary component is negative can only be matched by an L-network.

The matching network proposed for the HF tuner consists of a number of discrete components in each of the series and shunt arms of the network. At times using discrete components, the VSWR for the π-network can be significantly better than for the L-network over a large range of antenna reactances as shown in Fig. 6. The equations for computing the initial values of the components Ci, Co and L in π-network are presented in Section 7 under a description of the calculations performed by the microprocessor.

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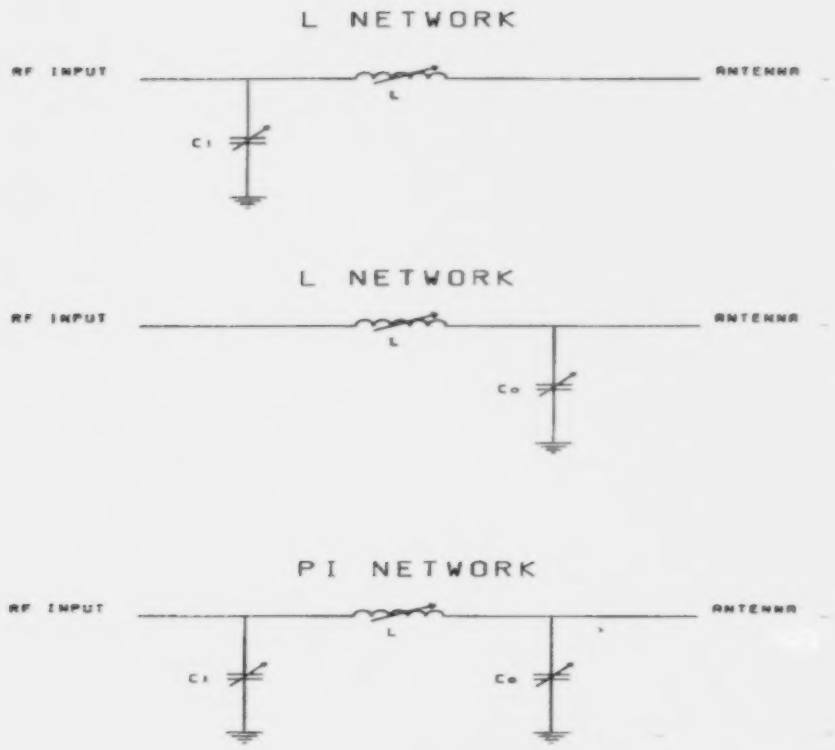


Fig. 5 L & PI NETWORK

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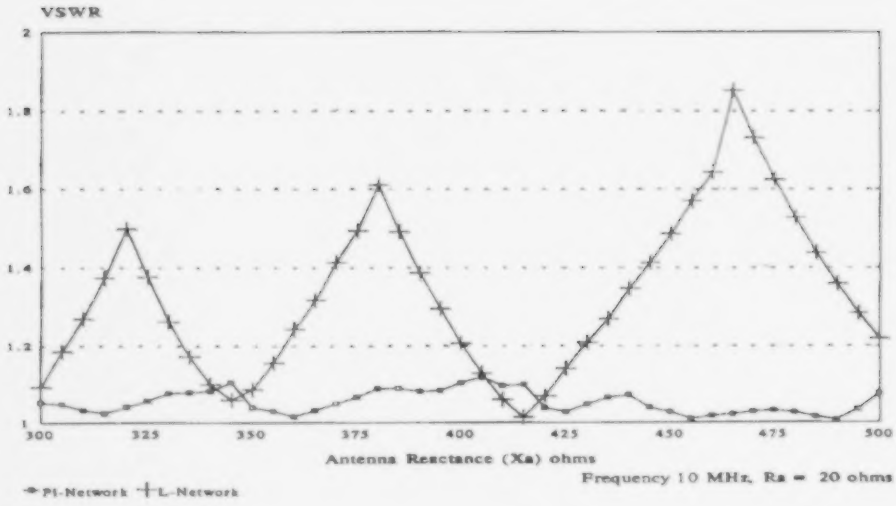


Fig. 6 VSWR OF PI NETWORK AND L NETWORK

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## 4.2 π-Network Configuration

The proposed π-network consists of a number of discrete components in each of the series and shunt arms of the network. Since the tuning of each arm is in discrete steps and not continuous, a minimum value of VSWR is only attainable due to the incremental values of inductance and capacitance proposed for the π-network. The larger the incremental steps in the inductance and capacitance the larger the VSWR. The smaller the incremental steps the smaller the VSWR but the larger the number of components required in the tuning network. The minimum VSWR attainable in a π-network for various incremental steps was computed for antenna resistances of 5, 50 and 1000 ohms and reactances varying from +750 to -750 ohms using a network analysis program developed by Petrie Telecom Ltd. This program automatically steps the component values in the π-network in specified incremental steps and selects the components that give a minimum value of VSWR. For a VSWR of about 1.6:1, the computations indicate the inductance needs to be varied in 0.1 uh increments and the capacitance in 12.5 pf increments. For a VSWR ≤ 1.9:1, the inductance needs to be varied in 0.1 uh increments and the capacitance in 25 pf increments.

The 0.1 uh increment in inductance and the 12.5 pf in capacitance are considered absolute lower limits physically realizable in the construction of a matching network. Stray capacitances of several picofarads are commonly expected to occur in the matching network. Minimum values of 0.1 uh and 12.5 pf have been used in automatic antenna tuners utilizing mechanical relays for switching in the various values of capacitance and inductance.

In order to minimize the number of inductors and capacitors required by the tuner, it is proposed that the binary set of elements shown in Table 1 be used in the π-network. For the binary set of elements, the incremental step size of each capacitor bank is 12.5 pf and the inductor bank is .1 uh. The maximum inductance and capacitance used in the π-network is greater than that required to match the impedance of the CRC antenna.

Table 1

| Ls uh | Ci pf | Co pf |
|---|---|---|
| 0.0 | 0.0 | 0.0 |
| .1 | 12.5 | 12.5 |
| .2 | 25 | 25 |
| .4 | 50 | 50 |
| .8 | 100 | 100 |
| 1.6 | 200 | 200 |
| 3.2 | 400 | 400 |
| 6.4 | 800 | 800 |
| | 1600 | 1600 |

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## 4.3 π-Network VSWR and Losses

In Appendix B are shown the minimum VSWR attainable and the matching network losses calculated for a matching network consisting of the component values of inductance and capacitance given in Table 1. The VSWR and losses were computed for antenna resistances of 5, 50 and 1000 ohms and reactances varying from +500, +250, 0, −250 and −500 ohms.

All calculations are based on an inductance with a Q of 125. Both losses in the inductor as well as the mismatch losses at the transmitter end of the network are taken into account in the calculations. An examination of the results in Appendix B reveals that the proposed π-network provides a VSWR ≤ 2.0:1. for the computed range of antenna impedances. The highest values of VSWR occur when the resistance = 5 ohms and the reactance = 0 ohms at 15 MHz due to the 0.1 uh increment in inductance being slightly large. An examination of matching network losses indicates that the tuner loss is maximum at the low values of antenna resistance when the reactances are large.

The measured values of antenna resistance and reactances for the CRC antenna at discrete frequencies over the frequency band from 2 to 15 MHz are shown in Table 2. An examination of impedance data in the Table reveals that the antenna reactance are less than a few hundred ohms when the resistance is about 5 ohms. The results in Appendix B indicate the π-network losses for a antenna resistance of 5 ohms and a reactance of ±250 ohms is less than 2 dB. Also Appendix A indicates the losses are less than 1.0 dB for antenna resistances of 50 and 1000 ohms and reactances of −500 and +500 ohms. These latter reactances correspond to the maximum values of reactance shown in Table 2. In general, it is concluded the losses in the matching network will not exceed 2 dB and generally be less than 0.5 dB for the CRC 3-wire antenna system.

Table 2

| Freq | Antenna Impedance | | Freq | Antenna Impedance | |
|---|---|---|---|---|---|
| MHz | Xa | Ra | MHz | Xa | Ra |
| 2.0 | 0 | 280 | 6.5 | -50 | 40 |
| 2.1 | -150 | 160 | 7.0 | 0 | 80 |
| 2.3 | -50 | 15 | 7.5 | -25 | 38 |
| 2.6 | 0 | 4 | 8.0 | 0 | 20 |
| 3.0 | 25 | 4 | 8.5 | 20 | 20 |
| 3.3 | 90 | 20 | 9.0 | 70 | 26 |
| 3.6 | 250 | 150 | 9.5 | 125 | 60 |
| 3.7 | 0 | 400 | 10.0 | 170 | 200 |
| 3.8 | -100 | 300 | 10.5 | 300 | 600 |
| 4.0 | 0 | 38 | 11.0 | -300 | 650 |
| 4.5 | 180 | 40 | 11.5 | -100 | 100 |
| 5.0 | 580 | 600 | 12.0 | -75 | 80 |
| 5.1 | 0 | 1180 | 13.0 | -10 | 20 |
| 5.2 | -580 | 600 | 14.0 | 50 | 55 |
| 5.5 | -200 | 80 | 15.0 | 140 | 38 |
| 6.0 | 0 | 60 | | | |
| 6.2 | 10 | 250 | | | |
| 6.3 | -150 | 45 | | | |

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## 4.4 Voltage and Current Ratings for Ls, Ci, and Co

The maximum current and voltage ratings for the elements of the π-network were computed based on the tuner being connected to the CRC 3-wire antenna. The maximum current in the series inductor Ls occurs when the antenna impedance is a minimum. The minimum impedance for the CRC antenna is 4 ohms resistive resulting in a maximum current of 15.8 amps for a transmitter power of 1000 watts. The inductors will be constructed of #16 AWG wire whose continuous duty current carrying capacity is rated at 22 amps for a single wire in open air environment. The #16 AWG wire shall be covered with a teflon sleeve rated with a peak breakdown voltage greater than 2000 volts. The cores of the inductor shall be constructed of Amidon iron powder cores (Material #2) with a $\mu = 8$.

The maximum RMS voltage across the input capacitors (Ci) is 316.2 volts based on an impedance of 100 ohms from the balun and a transmitter power of 1000 watts. The maximum RMS currents for the various capacitors proposed for the π-network are shown in Table 3. The maximum current flowing in the capacitor occurs at the highest operating frequency. The higher values of capacitances (1600) are only used for tuning at the lower frequencies and this has been taken into account in computing the maximum current. The Part No. refers to Murata Erie ceramic capacitors listed in their Catalogue No. 62-09. The size of the capacitors in the table refer to the dimensions of a cylindrical in which the first term is the height and the second term the diameter. For a capacitance of 1600, it is planned to connect 800 pf in parallel to obtain the desired values since larger capacitors with diameters as large as 4.5" are difficult to mount in a small volume.

Table 3
Current and Voltage rating of Ci

| Ci pf | Maximum Current | Part No. | Rated Current | Maximum Voltage | Size |
|---|---|---|---|---|---|
| 12.5 | .4 A | DCC510NPO250K | .9 A | 7.5 kV | .9"x.9" |
| | | DCC510NPO250K | .9 | 7.5 | .9"x.9" |
| 25 | .7 | DCC510NPO250K | .9 | 7.5 | .9"x.9" |
| 50 | 1.5 | DCC510NPO500K | 1.7 | 7.5 | .9"x.9" |
| 100 | 3.0 | DAU30N750101K | 7.0 | 1.5 | .9"x1.2" |
| 200 | 6.0 | DAU30N750201K | 7.0 | 1.5 | .9"x1.2" |
| 400 | 7.1 | DAU40N750401K | 8.5 | 1.5 | .9"x1.6" |
| 800 | 7.9 | DAU60N750801K | 14.0 | 1.5 | .9"x2.4" |
| 1600 | 11.4 | DAU60N750801K | 14.0 | 1.5 | .9"x2.4" |
| | | DAU60N750801K | 14.0 | 1.5 | .9"x2.4" |

The voltage across the output capacitors (Co) in the π-network varies with the antenna impedance. For the CRC antenna, the maximum voltage of about 1100 volts rms occurs at a frequency of about 5.1 MHz when the antenna impedance is 1,180 ohms. The maximum RMS currents for the various capacitors proposed for the π-network are shown in Table 4. The maximum current flowing in the capacitor occurs at the highest operating frequency. The higher values of capacitances (100, 200 and 400pf) are only used for tuning at the lower frequencies and this has been taken into account in computing the maximum current. As in Table 3 the Part No. refers to Murata Erie ceramic capacitors listed in their Catalogue No. 62-09. The rated maximum voltage refers to the peak voltage which is greater than the operating peak voltage (1100 x 1.4 = 1555 volts).

Table 4
Current and Voltage rating of Co

| Co pf | Maximum Current | Part No. | Rated Maximum Current | Voltage | Size |
|---|---|---|---|---|---|
| 12.5 | 1.3 A | DCC507NP0250K | 1.7 A | 15.0 kv | 1.1"x1.9" |
| | | DCC507NP0250K | 1.7 | 15.0 | 1.1"x1.9" |
| 25 | 2.6 | DAU40P100250K | 8.5 | 3.0 | .9"x1.6" |
| 50 | 5.2 | DAU40NPO500K | 8.5 | 3.0 | .9"x1.6" |
| 100 | 9.3 | DAU60NPO101K | 14.0 | 3.0 | .9"x2.4" |
| 200 | 8.3 | DAU80NPO201K | 18.0 | 3.0 | 1.1"x3.2" |
| 400 | 8.3 | DAU80NPO201K | 18.0 | 3.0 | 1.1"x3.2" |
| | | DAU80NPO201K | 18.0 | 3.0 | 1.1"x3.2" |

## 4.5 Variation of VSWR with Temperature

The variation of VSWR due to changes in the component values of the π-network with temperature was investigated to determine if any adjustments in tuning are required after the antenna is matched to the transmitter. Using the network analysis program, the VSWR was computed for specified variations in inductances and capacitance as shown in Appendix C. In all computations, Q=125 was assumed for the series inductance.

Discussions with Amidon indicate the percentage variation of inductance using iron powder cores (Material #2) with a $\mu$ = 8 is 0.4% for a temperature rise of 50°C. Variations of the series inductance by 5% have a small effect of the VSWR as shown in Appendix C-1. The capacitors Ci with Part No. starting with DCC have a temperature coefficient of 0±60 ppm/°C and with DAU a temperature coefficient of -750±120 ppm/°C. For a 50°C temperature variation, the capacitance shall vary a maximum of 4.3%. Variations of the input capacitance Ci by 5% have a small effect on the VSWR as shown in Appendix C-2 and C-3 for antenna resistance of 5 ohms and reactances of 0 and -250 ohms. All capacitors Co have a temperature coefficient less than 100±60 ppm/°C. For a 50°C temperature variation, the capacitance shall vary a maximum of ±

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0.8%. The variations of the input capacitance Ci by 3% have a small effect on the VSWR as shown in Appendix C-4 and C-5 for several typical values of antenna impedance. The variation of VSWR for other antenna impedances with larger resistive components are less than those shown in the Appendix C.

There is a requirement to operate the tuner continuously at a transmitter power of 1000 watts for a period no longer than 20 minutes. Once the transmitter is turned "off", it is assumed that it will not be turned "on" for at least 20 minutes. For these operational conditions, it is anticipated that the temperature rise will be less than 50° C and there will be no need to alter the tuning of the π-network due to variations of the components with temperature. The above conclusion assumes that the tuner matches antenna impedances similar in magnitude to those of the existing CRC antenna.

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## 5.0 PIN DIODE SWITCHES

### 5.1 General Description

PIN diodes will be used to switch the series inductor and shunt capacitors used in the matching π-network. An important property of the PIN diode is that its resistance can be varied from a fraction of an ohm to more than 10,000 ohms with a DC control current. When the DC current is switched "on" and "off", the diode can insert or remove a component in the matching network.

The RF power handling capability of PIN diode switches is limited either by thermal considerations or a voltage breakdown of the diode. M/A-COM Inc is a main manufacturer of high power PIN diodes. The power dissipation ($P_D$) at 25°C and maximum instantaneous breakdown voltage ($V_{BR}$) of the following types of PIN diode are as follows:

| Type | $P_D$ watts | $V_{BR}$ volts |
|---|---|---|
| MA4PK2001 | 50 | 2000 |
| MA4PK3001 | 75 | 3000 |

In order to turn the PIN diode switch "On" requires a DC forward current of about 200 ma and at this bias the series resistance of the PIN diode is about 0.2 ohms. For the maximum operating RF current of about 14 amperes in the inductors and capacitors presented in Section 3.2.4., the maximum power dissipation in the PIN diode is about 40 watts assuming losses in the inductor with a of Q=125. The MA4PK3001 PIN diode with a rated power dissipation of 75 watts is capable of handling the 40 watts dissipation.

### 5.2 Required DC Negative Bias

In order to maintain the diode switch in the "Off" position requires a DC negative voltage due to a self generated DC voltage by the PIN diode. The DC negative voltage required to prevent the diode from conducting is given by the following expression

$$V_{dc} = V_{rf}/[1+(0.0285fW^2/V_{rf})^2]^{\frac{1}{4}}$$

where $V_{rf}$ = peak RF voltage
$f$ = frequency in MHz
$W$ = i-region thickness of the diode in mils

The i-region thickness of the MA4PK3001 PIN diode is 325 um or 13 mil. The maximum peak-RF-voltage ($\sqrt{2}$ Vrms) across the tuning capacitors Ci is 316 volts, Co is 1,555 volts and across the series inductor Ls is 1,240 volts. The values of $V_{dc}$ for various frequencies and peak RF operating voltages are as follows:

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| Frequency | Peak RF voltage | $V_{dc}$ |
|---|---|---|
| 2.0 MHz | 316 volts | 316 volts |
| | 1,240 | 1,240 |
| | 1,555 | 1,555 |
| 15.0 | 316 | 308 |
| | 1,240 | 1,237 |
| | 1,555 | 1,553 |

The above results indicate that a negative DC bias equal to the peak voltage is required to switch off the PIN diodes. Undef these conditions a current less than a milliamp is required due to the high resistance of the diode when negatively biased.

The maximum RF voltage across the PIN diode will be the sum of the DC bias voltage plus the peak RF operating voltage. For the series inductor Ls and the capacitances Ci and Co, the maximum operating voltages are as follows:

| Element | Maximum Operating Voltage |
|---|---|
| Ls | 2,480 volts |
| Ci | 632 |
| Co | 3,110 |

The MA4PK3001 PIN diode has a rated instantaneous breakdown voltage of 3,000 volts. For the series inductor Ls and the capacitor Ci a single pin diode is within rated specifications. However, the capacitor Co requires the use of two PIN diodes in series in order not to exceed the rated specifications.

**5.3 PIN Diode Circuits**

The proposed PIN diode circuits for switching a series inductor $L_s$ and two shunt capacitors $C_o$ across the balanced feed line are shown in Fig. 7. The driver circuitry in not shown in Fig. 7. RF chokes L2, L3, L4 and L5 enable the passage of DC current and blocks the RF signal entering the driver circuitry. Capacitor C2 equalizes the currents in the PIN diodes. For the series inductor switch, blocking capacitors may be required to prevent flow of DC bias currents into the antenna system.

A simple switch using a single PIN diode was constructed to measure its isolation. The measured variation of the isolation of this switch with frequency is shown in Fig. 8 for an RF input of around 200 volts. The PIN diode circuit shows the isolation is greater than 48 dB between 2 and 15 MHz when the switch is in the "off" position. A PIN diode switch was switched "off " and "on" at a low RF power levels of 125 watts for several days with out any noticeable degradation. A driver circuit was designed and built to apply 6 volts to turn "on" the switch and -700 volt to turn "off" the switch. With this simple driver circuit the PIN diodes was able to be switched "off" in about 75 usec and switched "on" in about 40 usec.

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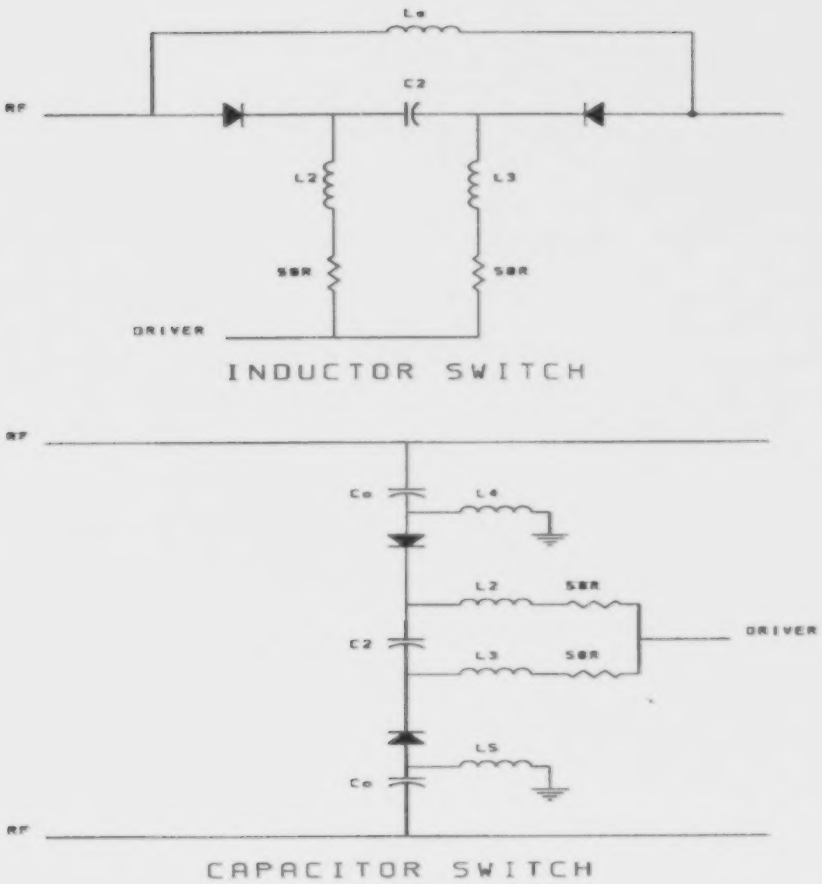


Fig. 7 PIN DIODE SWITCH

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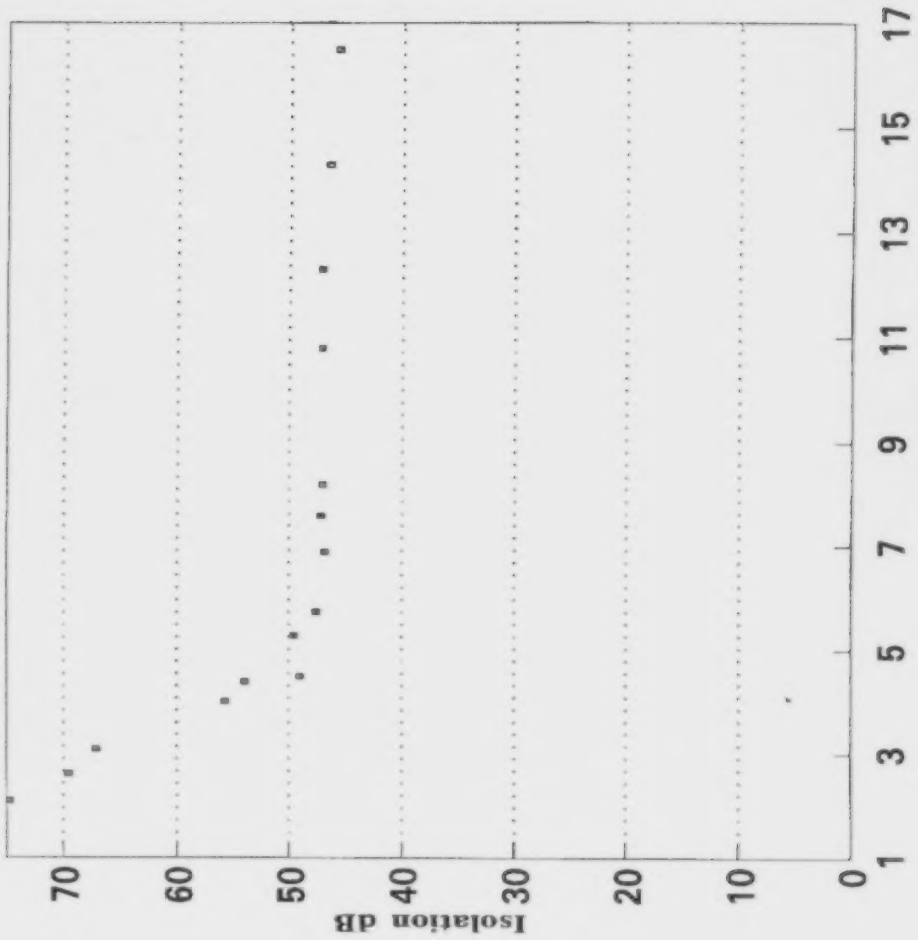


Fig. 8 PIN DIODE ISOLATION

The test driver circuit was not suitable for switching at higher voltage levels since the semiconductors exceeded their voltage ratings. To solve this problem and also decrease the switching time by a factor of at least 4, a new driver circuit was designed as shown in T-11004. In this driver circuit each switch consists of two Vmos devices in series (S1 consists of Q2 and Q3: S2 consists of Q4 and Q5) with 800 V zeners between drain and source to equalize the voltages. 20V zeners are connected from the gate to the source to protect the gate from transients. Q2 and Q3 operate in an unusual manner, since the control signal only goes to Q3. When Q3 is turned on, it's drain pulls down the source of Q2 so that D4 conducts and turns on Q2. Q4 and Q5 only operate in pulsed mode, so their gates are driven by pulse transformer T1.

When the fibre optic receiver U2 receives a light signal from the transmitter it turn on S1 via U1A which turns on the pin diodes via the 50Ω resistors. When the light signal disappears, monostable U3 generates a 10 usec pulse to turn on S2 via Q1 and T1. This pulse pulls the charge out of S1 and the pin diodes. After the pulse the 270 kΩ resistors across Q4 and Q5 keeps the output at +1.2kV. The resistors R1 and R2 between Q2 and Q5 limits the peak current to about 130mA. The supply voltages are +1.2kV and -15V. Light emitting diode D9 provides a visible indication of driver operation.

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## 6.0 DIGITAL CONTROLLER

The digital controller provides both an input and output data interface with the computer via the AT bus of a 486 microcomputer. A block diagram of the digital controller system is shown in Fig. 9. The controller receives serial input data from the A/D converter and converts this data to a parallel format that is accepted by the AT bus. The controller receives control signals from the microcomputer that both initiates a request for measurement signal and sets the state of the PIN diode switches. An AT bus I/F & I/O decoder is used to connect signals between the AT bus of the microcomputer and the input/output lines of the digital controller.

A detailed schematic of the circuitry in the digital controller is shown in five diagrams labelled T-11005. In diagram T-11005/1, U13 and U14 are address buffers, and U11 and U12 are data bus buffers. S1 is a DIP switch which sets the I/O address of the card, nominally set to 0300 Hex, the standard address for prototype cards assigned by IBM. U10 compares the address from S1 with the buffered bus address. The /IOS signal goes low when the address is in the range 0300 to 030F hex. U5 decodes I/O writes strobes, and U6 decodes I/O read strobes. This interface card only accepts word (16-bit) I/O operations, not byte operations. All I/O addresses are even. /IOR0 is 0300, /IOR1 is 0302 etc. /IOW0 is 0300, /IOW1 is 0302, etc.

In diagram T-11005/2, U16 through U21 are latches to control the RF PIN diodes via a fiber optic link. Two sets of 16-bit latches are required for 32 lines. U16 and U17 are first loaded (0300 hex) and then U18 and U19 (0302 hex). All 32 bits (LED1 through LED32; T-11006/1&2) are updated simultaneously when U18 and U19 are loaded. U20 and U21 transfer data loaded in U16 and U17 when U18 and U19 are activated. In diagram T-11006/1&2, Lines LED1 through LED32 interface to fiber optics LED transmitters in an external box via connector J1.

In diagram T-11005/2, U15 is a monostable that generates about a 4 usec pulse when an IOW2 (0304 hex) instruction is issued. This pulse requests data from the A/D interface box. The remainder of the AT interface card receives 10 MBPS serial data from the A/D interface box. A fiber optic receiver (MFOD2405:T-11007) connects to the AT interface card via a short cable.

In diagram T-11005/4, U48 provides a stable clean voltage (+5V) to the receiver. U30 is a high speed comparator which converts the analog signal from the fiber optics receiver (a PIN photodiode and transimpedance amplifier) to logic levels. R8 sets the threshold level (about 0.8 volt). R5 and R6 provide hysteresis, avoiding high frequency oscillation when the signal is near the threshold. The serial data is asynchronous NRZ (non-return to zero). A data frame begins with a start bit (logic HI), followed by 73 data bits (LSB first), and a stop bit (logical LO). Assuming U2A is cleared

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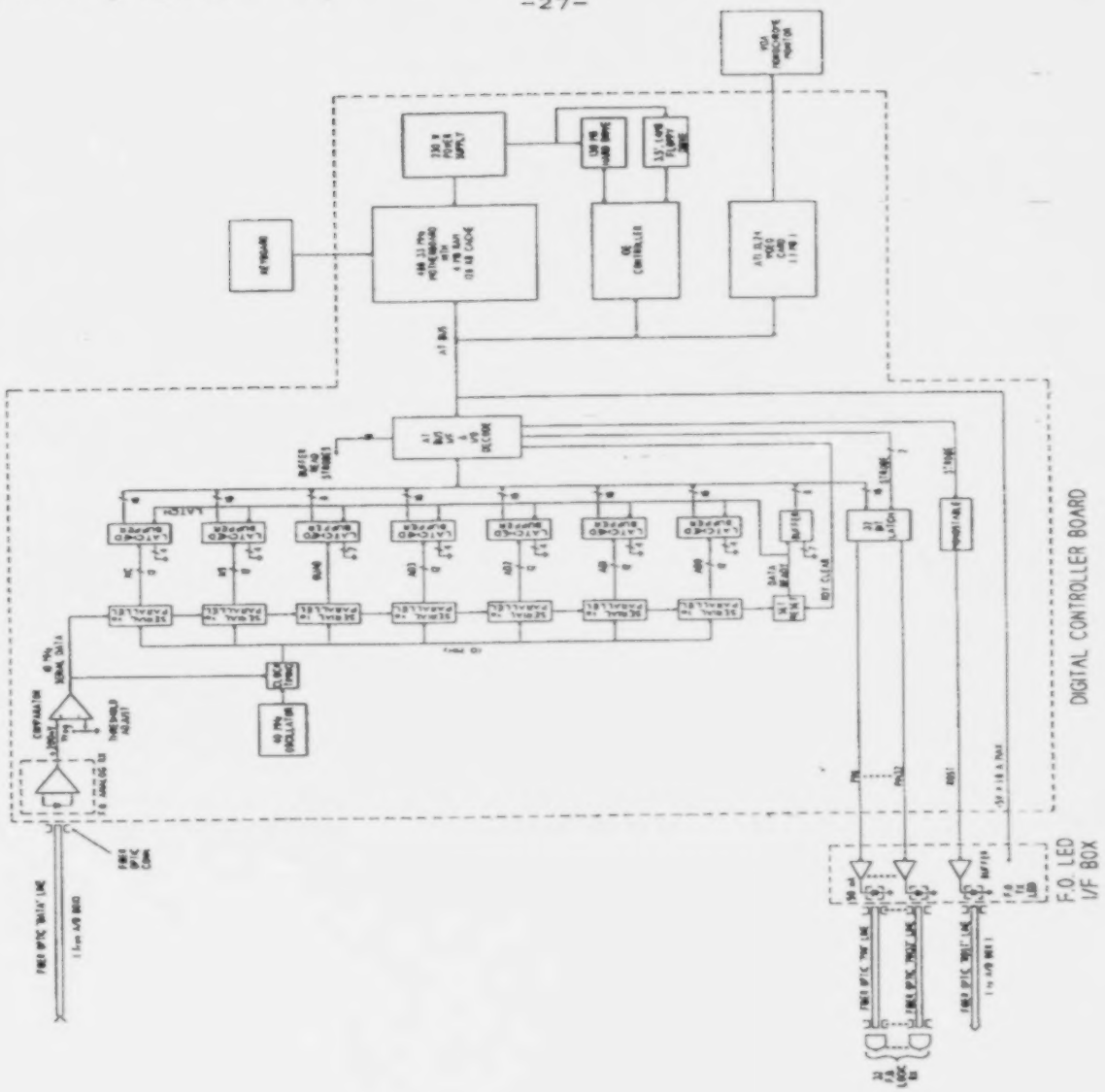


Fig. 9 BLOCK DIAGRAM OF DIGITAL CONTROLLER SYSTEM

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by an IOW3 strobe (0306 hex), U2A is set on the leading edge of the start bit. U2B synchronizes the output of U2A to the next falling edge of the 40 MHz clock (four times the data rate). U1A and U1B form a divide by four divider. As U1 is synchronized by U2B, the 10 MHz SERCLK signal has its rising edges near the centre of the serial data (SERDAT) bits.

In Diagram T-11005/3, SERDAT clocks shift registers U22, 23, 24, 34A, 31, 32, 33, 35, 36, 38, and 34B. The output of U37A goes high when all 73 data bits have been received, setting U37B and latching the data into latches U25, 26, 27, 28, 29, 39, 40, 41, 42, 44, 45, 46, and 47. Bit 15 (MSB) of I/O address 030E hex is the "data ready" bit. I/O read addresses 0300 through 030C hex can then access the data when the ready bit is set. The ready bit is reset via an I/O write strobe to 0306 hex. All data is right justified 16-bit format. A 12-bit A/D words has the upper 4 bits set to zero.

The AT interface card is connected to the fiber optics LED interface box via a 37-pin ribbon cable. This cable carries 32 control bits, the RQST pulse, and power and ground. The interface box uses emitter follower transistors to provide drive current to the fiber optic IR LEDs. Series resistors set the drive current to about 50 mA. If all 32 LEDs are turned-on, the total drive current could reach about 1.6 A. Power for the LEDs is derived from the computer power supply.

## 7.0 MICROPROCESSOR

### 7.1 General Description

The microprocessor unit processes the data sent from the RF measurement unit and computes the following items:

- Compute the initial values of capacitance and inductance for the matching network based on measurements of the antenna impedance and operating frequency.
- Compute the "final" values of capacitance and inductance based on measurements of the impedance at the input to the tuner.
- Store the "final" values of capacitance and inductance for at least 20 operating frequencies.
- Check if the operating frequency has previously been used and if so, select the stored information on the values of capacitance and inductance.

The microprocessor also provides output data to select the appropriate PIN diode drivers in the π-matching network and various control signals to operate the RF measurement circuits. A listing of the programs to test this portion of the system including the fiber optic link is operational is given in Appendix F.

### 7.2 Computation of Initial Capacitances and Inductances

The basic equations given in 7.2.1 and 7.2.2 will be used to compute the initial values of inductance and capacitance for matching a transmitter with an input resistance Ro to the antenna. These equations are relatively simple and should enable the initial component values to be computed quickly. Resistive losses in the series inductance are taken into account in the equations by assigning a value of Q=125 to the inductive elements.

#### 7.2.1 For Ra ≤ Ro ohms

If the antenna resistance (Ra) is less than the transmitter resistance (Ro), the capacitive reactance of the π-network at the transmitter end (Xi) is given by the following expressions:

$$Xi = -Ra[Ra/(Ro-Ra)]^{\frac{1}{2}} \quad \text{.... 1}$$

and the series inductance by:

$$Xs = -(RoRa/Xi)-Xa \quad \text{.... 2}$$

where

Ro = transmitter resistance of 50 ohms
Ra = antenna resistance
Xa = antenna reactance

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For the series inductance obtained from equation 1, the resistance in the coil is computed based on a Q=125. This resistance is taken into account in the calculations by including this resistance as part of the antenna load resistance.

**7.2.2 <u>For Ra ≥ Ro ohms</u>**

If the antenna resistance (Ra) is greater than the transmitter resistance (Ro), the capacitive reactance of the π-network at the antenna (Xo) is given by the following expression:

$$Xo = \frac{RoXa - [(Ro)^2(Xa)^2 + Ro(Ra-Ro)(Xa^2+Ra^2)]^{1/2}}{Ra-Ro} \quad \ldots.3$$

where
- Ro = transmitter resistance
- Ra = antenna resistance
- Xa = antenna reactance

The impedance of the parallel combination (Rp + jXp) of the antenna impedance and capacitance is given by the following expressions:

$$Rp = RaXo^2/[Ra^2+(Xo+Xa)^2]$$

and

$$Xp = Xo[Ra^2+Xa(Xo+Xa)]/[Ra^2+(Xo+Xa)^2] \quad \ldots.4$$

The resistance (Rp) computed using equation 4 is equal or less than 50 ohms. For this impedance the series inductance and input capacitance can be computed using expressions 1 and 2 for Ra ≤ Ro. Equations 1 to 4 can also be used to compute the elements of a π-network for conditions where Ra ≤ Ro and Xa ≤ 0 when the value under the square root in equation 4 is not less than zero.

A computer program written in C language was developed to compute the value of the components in the π-network using the above equations. This program was implemented in an PC computer to select the initial values of the components. The flow chart and the C language program to do the calculations are shown in Appendix D. The initial VSWR expected using the basic equations was calculated using a network analysis program and are presented in D-3 to D-5. For these calculations the π-network was based on the incremental steps of 0.1 uh values for inductance and of 12.f pf for the capacitance. The inductance losses in the matching network were accounted for by assuming a "Q" of 125. These equations seem to be appropriate for computing the initial values of inductance and capacitance.

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## 7.3 Computation of Final Capacitances and Inductances

A method was developed that will quickly adjust the initial values of inductance and capacitance to their final values corresponding to a minimum VSWR. The initially selected values will be in error due to:

- the assumptions in the equations and the simplicity of the method used to select the component values. For example Q= 125 for the inductor and the approximate method for taking into account the resistance in the coil.
- inaccuracy in the component values of the inductance and capacitance.
- neglecting lead inductance and stray capacitance.
- losses in the PIN diode switches
- errors in the measurement of the forward and reflected voltages (Vf and Vr) and the angle $\Phi$ associated with the complex antenna impedance Za.

The method proposed to adjust the initial values of inductance and capacitance to their final values is based on the following measurements of VSWR and computations of values for the components in the matching network. Fig 10 shows a pictorial representation of the overall method and the situation where there is no change in the component value.

a) For the initial computed values of Ls, Ci and Co measure the VSWR (labelled $VSWR_a$) at the input to the tuning network.

b) Alter the components in the matching network as follows:
   - adjust Co, then Ls and then Ci

c) Smallest incremental values of components are:
   for Co and Ci = 12.5 uf
   L = 0.1 uh

d) Compute an initial estimated component offset factor based on the current VSWR:

   $PSKIP = 0.14 \ln (VSWR_a/0.993)$, with an upper limit of 0.20

e) For the order of the components presented in paragraph b), compute two new adjusted values rounded to the nearest incremental value:

   $Co \pm Co * PSKIP$

   For components Ci and Ls replace Co in the above expression by the corresponding variable.

If the magnitude of the change in component value is less than the smallest incremental value for that component, no further adjusting is necessary for that component. Select the next component in order as defined in paragraph b) and continue on.

f) Switch the two values computed in paragraph e) into the tuner network and measure the VSWR for these two values. Designate $VSWR_l$ and $VSWR_r$ as the measured left and right VSWR.

g) Compare $VSWR_l$ and $VSWR_r$ with $VSWR_m$. $VSWR_m$ is the value measured using the initial or middle value of the component.

If $VSWR_m > VSWR_l$ or $VSWR_r$ then select the value of the component with the lowest VSWR. Use the + sign in the equation if the VSWR is decreasing as the component value increases and the - sign if the VSWR is increasing as the value of the component increases.

If both $VSWR_l$ and $VSWR_r$ are greater than $VSWR_m$ then reduce PSKIP by one quarter and repeat paragraphs e), f) and g).

h) Repeat measurements and computations presented in paragraphs d), e), f) and g) for other components in the matching network in the order defined in paragraph b). Final adjustment of components is complete when one of the following conditions are met:

- After completing a round of adjusting Co, Ls, and Ci the change in VSWR is negligible (ie. < .01).
- The maximum number of allowable component changes/VSWR measurements has been reached ( ie. 10 changes max. ).
- VSWR is within acceptable limits. ( ie. < 1.6 )

### 7.4 Number of Tuning Steps

A computer program written in C language was developed to compute the final values of the components in the matching network using the above method. The C language program to determine the final values of the components in the matching network are shown in Appendix E. Using this program and the network analysis program for computing the VSWR, the final VSWR was computed for 10 and 20 tuning steps for the following combination of component inaccuracies and measurements errors:

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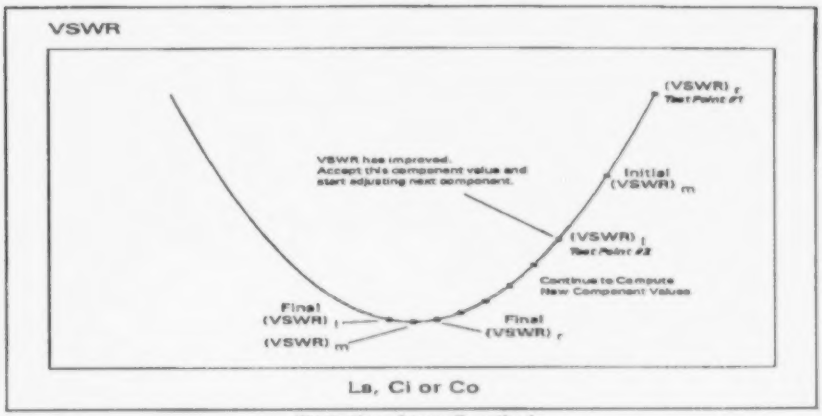


Illustration of overall method

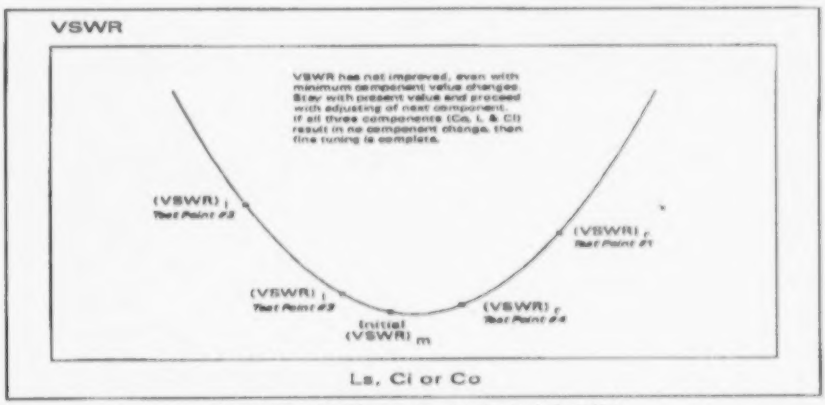


Illustration of a 'No component change' situation

**Fig 10. Method of Computing Final Values of Ls, Ci and Co**

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| | Ci | L | Co |
|---|---|---|---|
| Component Inaccuracies | 0% | 0% | 0% |
| | ±3% | ±3% | ±3% |
| | ±10% | ±10% | ±10% |
| | Z | Φ | |
| Measurement errors | ±5% | ±5° | |
| | ±10 | ±5° | |

The results of these calculations are shown in Figure 11 for the network matching the CRC antenna impedances. The maximum, minimum and average values of VSWR expected are shown for 10 and 20 tuning steps assuming the above combination of component and measurement errors. The maximum VSWR occurs around 3 MHz and is less than about 1.75:1 for 10 tuning steps. At 3 MHz the impedance of the CRC antenna is 4 + j25 ohms. This maximum does not decrease appreciably as the number of tuning steps is increased to 20. The maximum VSWR is mainly due to the ±5° error in the measurement of the complex impedance angle Φ. The method takes an average of 4 and a maximum of 14 adjustments of the network to tune to a VSWR ≤ 1.6:1 assuming a systematic error of ± 5% in all component values in the π-network.

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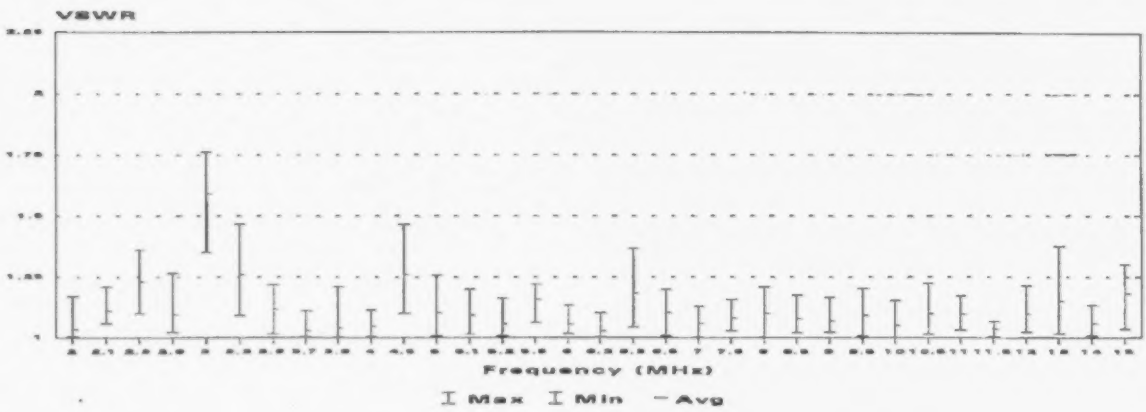


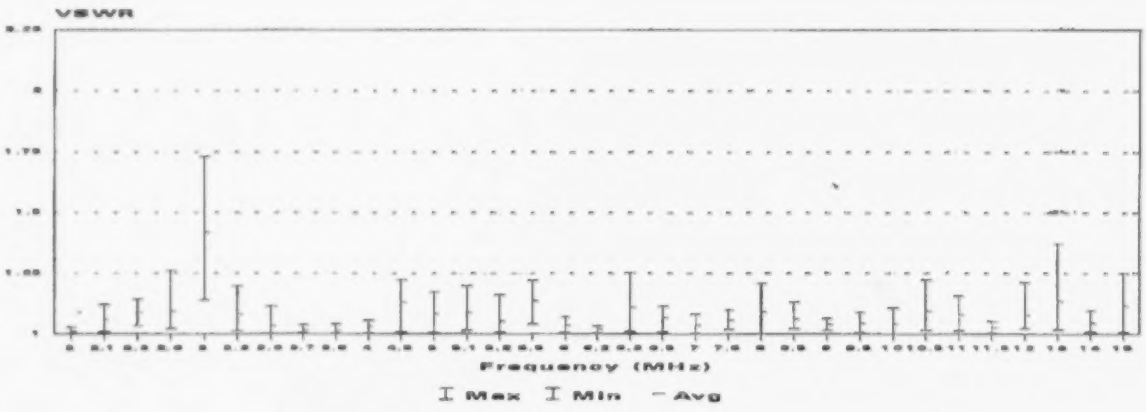


Fig 11. VSWR After 10 and 20 Fine Tuning Steps

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## 8.0 OPERATING SPEED OF TUNER

The length of time taken to match the antenna when the frequency is altered was a major concern in the design of the tuner. The faster the speed in matching the antenna to the 50 ohm output impedance of the transmitter, the less the heat dissipated in the tuner matching network and the shorter the presence of high voltage across the components and the PIN diodes.

Every time the components in the π-network are altered, the length time of taken from the start to the end of the change in components is a sum of the following items:

| | |
|---|---|
| a) Measurement of $V_{FWD}$ and $V_{REF}$, phase and frequency | 12 usec |
| b) A/D conversion and microprocessor control of RF measurements | 21 |
| c) Operation of PIN diode switch | 40 |
| d) Microprocessor calculation of component values in the π-network | 15 |
| Total | 88 usec |

The time for item a) is based on timing diagrams for the RF measurement system and item b) on actual operation of the A/D converter under microprocessor control. The time for the PIN diode switch is based on measurements using a test driver circuit and extrapolating the results to the final driver circuit proposed in this report. The microprocessor calculations in item d) is a weighted average of the time for the computation of the initial values of the components in the π-network and the time to compute the components using the final tuning algorithm described in Section 7.3.

The maximum number of tuning steps required to match the CRC antenna to the transmitter was reported in Section 7.4 to be about 10 steps. For 10 steps, the maximum time to tune to a new frequency is estimated as 88 usec x 10 = 880 usec or less than 1 millisecond.

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## 9.0 STATUS OF TUNER DEVELOPMENT

### 9.1 Work Completed

The following development work was completed under this contract:

- An analogue RF measurement system was designed that provides parameters to compute the signal frequency, the VSWR and the complex impedance at the input terminals to the antenna system.
- For the RF measurement system, a "breadboard" level detector circuit which provides a logarithmic output proportional to the RF input voltage was built and tested to check its linearity and variation with frequencies at 2 and 15 MHz.
- A π-network was designed and the components of the network specified to match the 50 ohm output impedance of the transmitter to the impedance of a balanced transmission line feeding the CRC antenna.
- For the π-network based on inductances with Q = 125, a network analyses program indicated the losses in the matching network will not exceed 2 Db and generally will be less than 0.5 dB for the CRC 3-wire antenna.
- A "breadboard" PIN diode circuit capable of handling 125 watts was tested for several days without any degradation in performance. The PIN diode was able to be switched "off" in about 75 usec with the isolation greater than 45 dB and switched "on" in about 40 usec.
- An improved PIN diode circuit capable of handling RF power of 1000 watts CW was designed to switch the components "off" and "on" in less than 40 usec.
- A fiber optic link was designed and tested that sends data from the RF measurement system to the microprocessor and also data to control the operation of the PIN diode switches.
- A digital controller was designed and tested that provides an input and output data interface with the AT bus of a 486 microcomputer.
- Equations have been derived and computer programs written and tested to compute the initial values of the capacitance and inductance for the π-network base on data from the RF measurement system.

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- A fine tuning method has been developed and computer programs written and tested to quickly adjust the initial values of inductance and capacitance to their final values corresponding to a minimum VSWR. The maximum number of steps required to match the CRC antenna to the transmitter is about 10 steps.

## 9.2 Work Required to Complete Tuner

The following work needs to be completed before an operational antenna tuner is available for testing:

- For the RF measurement system, prototype circuit boards need to be constructed and tested which measure the signal frequency, and the phase between the forward and reflected power.
- Thermal and mechanical design of π-network, then the assembly, and testing of the π-network.
- For the PIN diode switch, prototype circuit boards need to be constructed and tested with 1000 watts of RF power.
- Design of the layout, construction and testing with moderate power of an integrated circuit board containing the digital controller, microprocessor and RF measurement circuits.
- Integration and assembly of all systems into one or two units and testing with full RF power.

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## 10.0 CONCLUSIONS

The research and development contract resulted in the design of a tuner to match an efficient antenna developed at the Communications Research Centre. Much development work was done on the PIN diode switches and the matching π-network. Circuit boards have been built to test the operation of the PIN diode switches, the digital controller interfaced to a 486 microcomputer and some RF measurement circuits. Both the design work and the testing of the "breadboard" circuits indicate it is feasible to develop a tuner with the following specifications:

| | |
|---|---|
| Operating Frequency Range: | 2 to 15 MHz |
| RF Power Rating: | 1000 watts PEP continuous |
| Type of Switching: | Solid State |
| Tuning Time: | ≤ 1 msec |

The tuner designed under this contract has the following unique features:

- RF measurement system to determine the antenna impedance, operating frequency and VSWR,
- Microprocessor to compute the tuning components required in the matching network,
- Solid state PIN diodes to switch the tuning components in the matching network.

## 11.0 REFERENCES

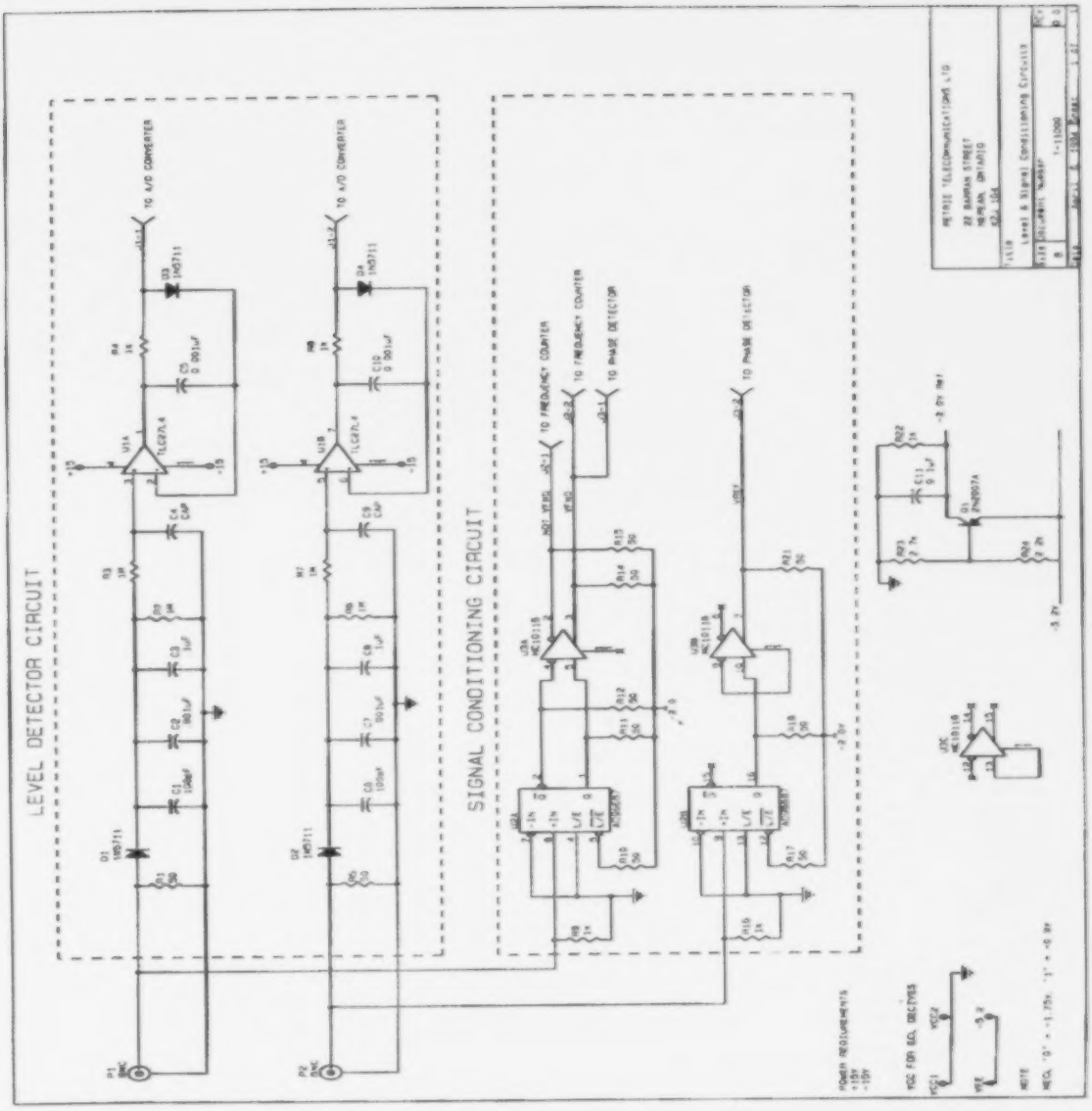
1. Design and Development of a Microprocessor Measurement and Control System for an Automatic HF Antenna Tuner. Diversitel Communications Interim Report, 27 July 1992.

2. Grebenkemper, J. The Tandem Match - An Accurate Directional Wattmeter. QST, January 1987.

3. Hiller, G. Design with PIN Diodes, MACOM Semiconductor Products Division, Report AG312.

4. Hiller, G. Predict Intercept Points in PIN Diode Switches, Microwaves & RF, December 1985.

# LIST OF SCHEMATIC DIAGRAMS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SIGNAL CONDITIONING CIRCUIT
TO A/D CONVERTER
TO A/D CONVERTER
TO FREQUENCY COUNTER
TO FREQUENCY COUNTER
TO PHASE DETECTOR
TO PHASE DETECTOR
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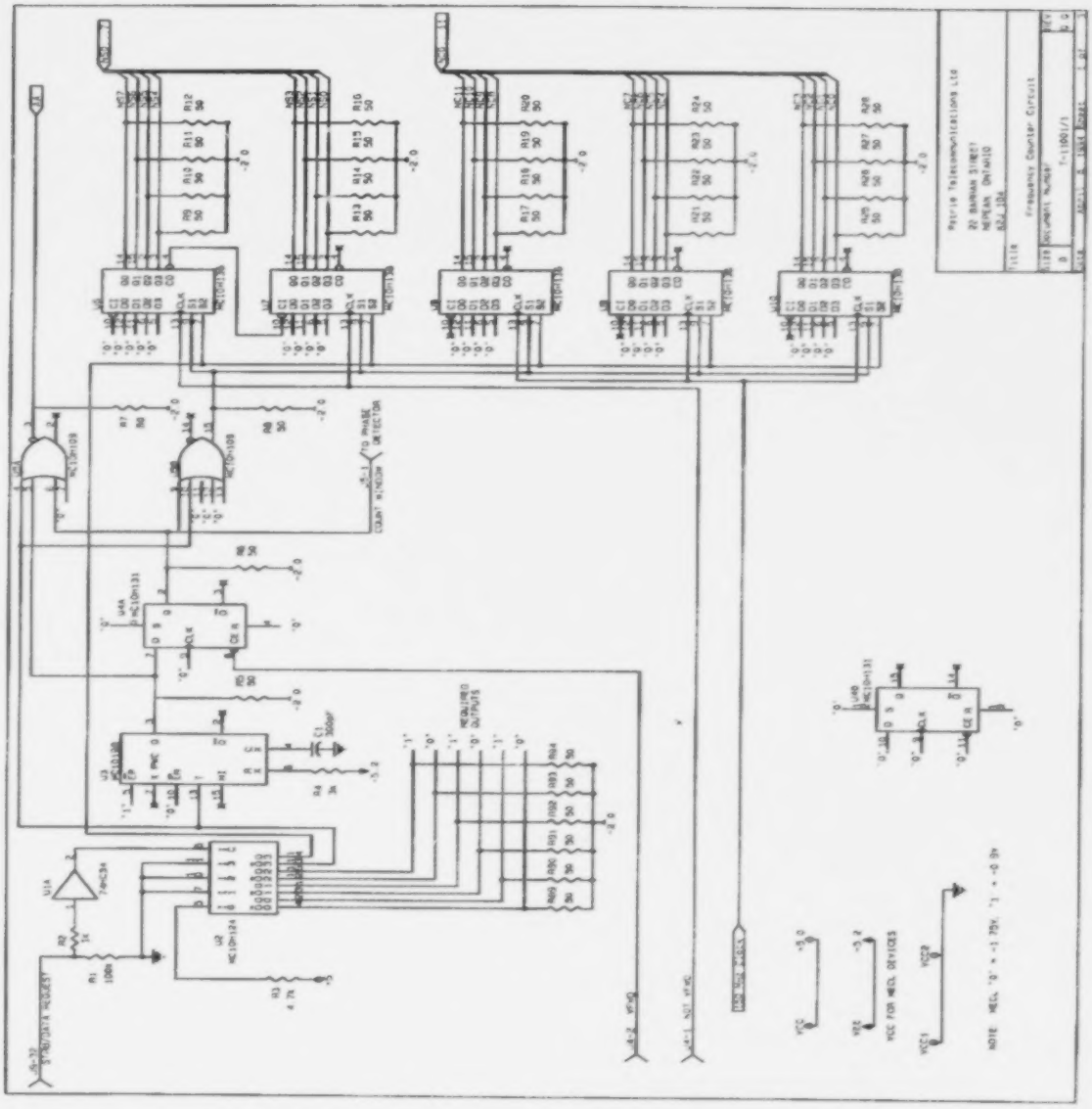
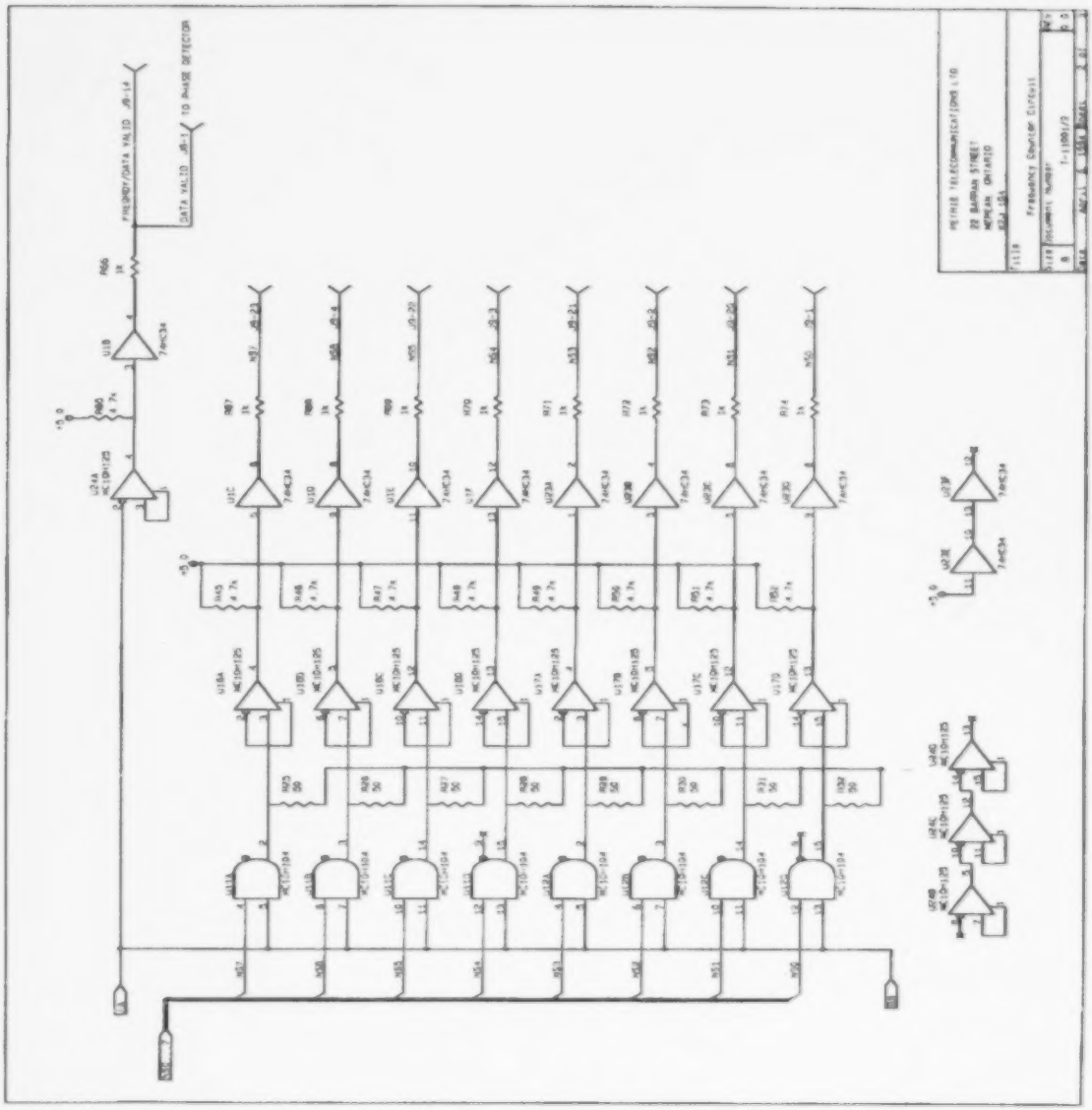
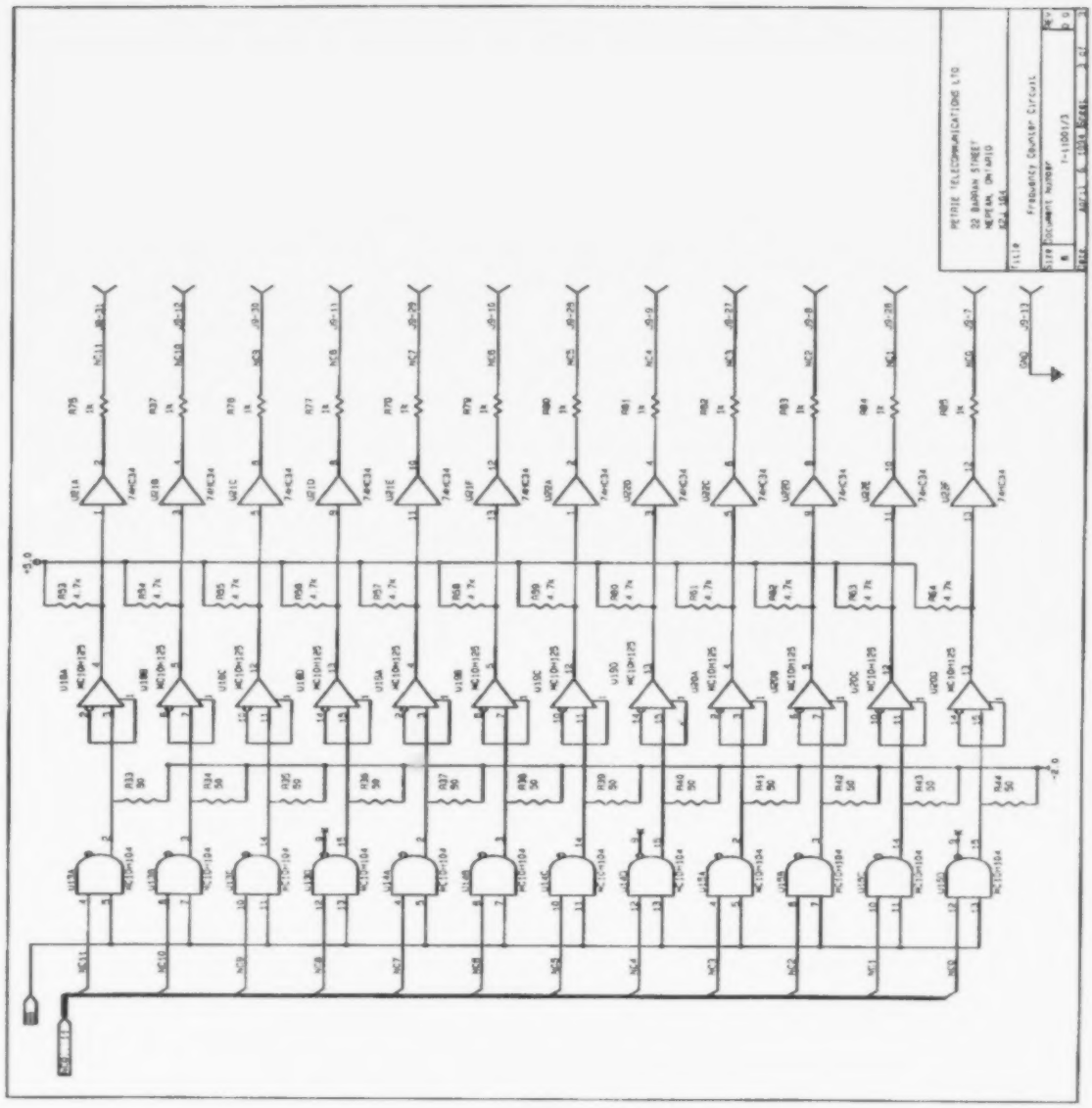
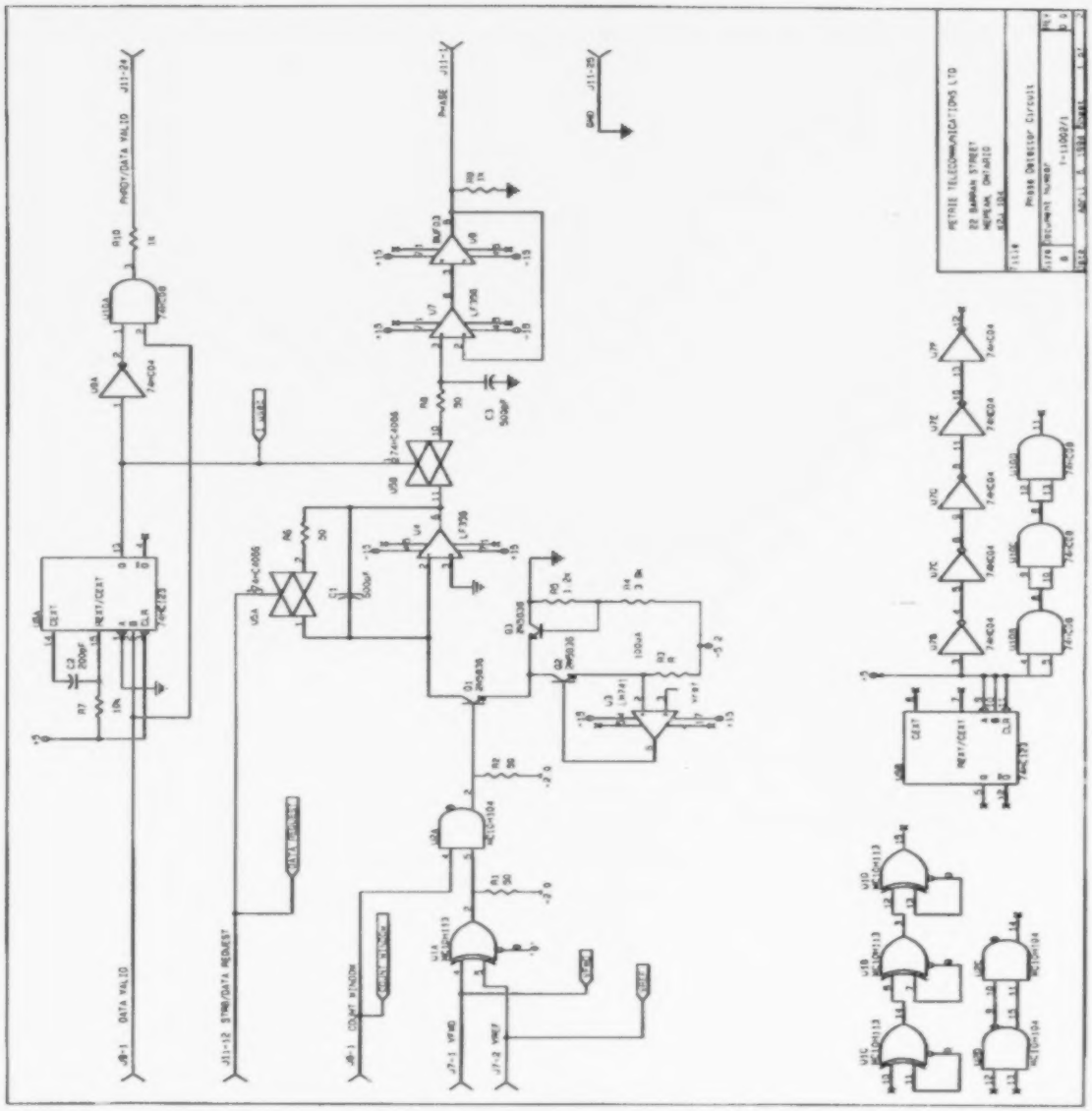
1N4711
1N4711
1N4711
TL074CN
TL074CN
MC10116
MC10116
MC10116
2N6027A
METRIZE TELECOMMUNICATIONS LTD
22 BARRAN STREET
NEPEAN, ONTARIO
K2H 1B4
Level & Signal Conditioning Circuits
POWER REQUIREMENTS
+15V
-15V
VCC FOR ECL DEVICES
VCC1
VCC2
-5.2
VEE
-5.2V


Paris Telecommunications Ltd
22 Barrow Street
Norman Ontario
K2J 3J4
Frequency Counter Circuit
MC10H109
MC10H131
MC10H104
MC10H116
PROGRAMMED OUTPUTS
TO PHASE DETECTOR
NOTE: MECL '0' = -1.75V, '1' = -0.8V






PETRIE TELECOMMUNICATIONS LTD
22 BARBAN STREET
PETRIE, ONTARIO
K2J 1B4
Phase Detector Circuit
DATA VALID
STRB/DATA REQUEST
COUNT WINDOW
VCO
74HC4066
74HC04
74HC86
74HC08
74HC00
74HC123
74HC74
74HC157
74HC153
74HC139
74HC373
74HC245
74HC688
74HC4040
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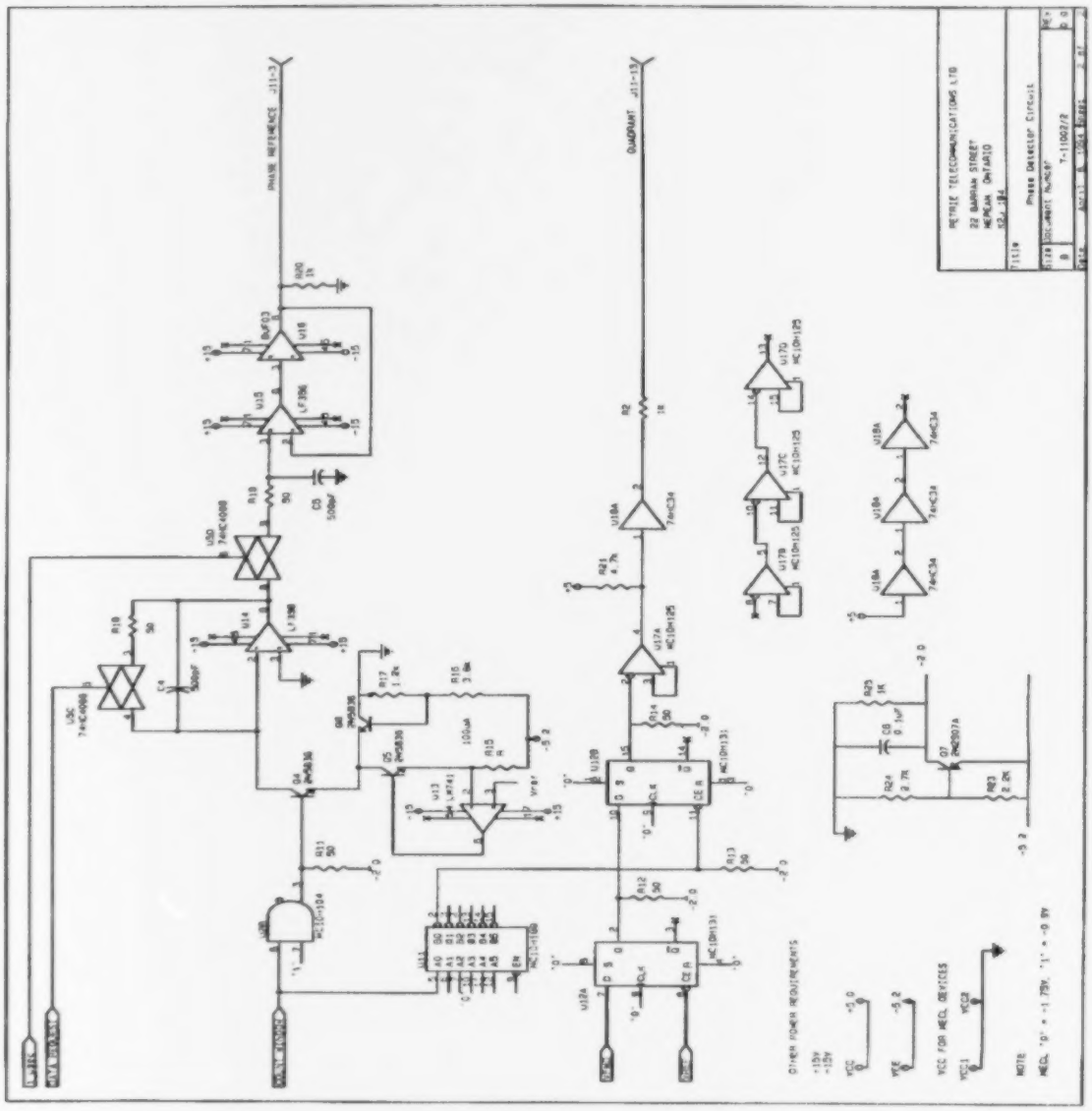
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R21 4.7k
R19 50
C3 5000pF
R18 50
C4 5000pF
R17 1.2k
R15 3.9k
R16 A
100uA
R14 50
R13 50
R12 50
R11 50
R23 1k
C8 0.1uF
R24 2.7k
R22 2.7k
Q7 2N2907A
Q8 2N5836
Q5 2N5836
Q4 2N5836
U8 74HC4066
U9 74HC4066
U14 LF356
U15 BUF03
U13 LM741
U12A 74HC34
U12B 74HC34
U12C 74HC34
U17A MC10H125
U17B MC10H125
U17C MC10H125
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U18B MC10H131
U19 MC10H131
U24 MC10H131
U11 MC10H104
U10 MC10H166
PETRIE TELECOMMUNICATIONS LTD
22 BARRAN STREET
MARKHAM ONTARIO
Phase Detector Circuit
DISCRIMINANT MONITOR
T-110021/2
OTHER POWER REQUIREMENTS
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-12V
VCC FOR MECL DEVICES
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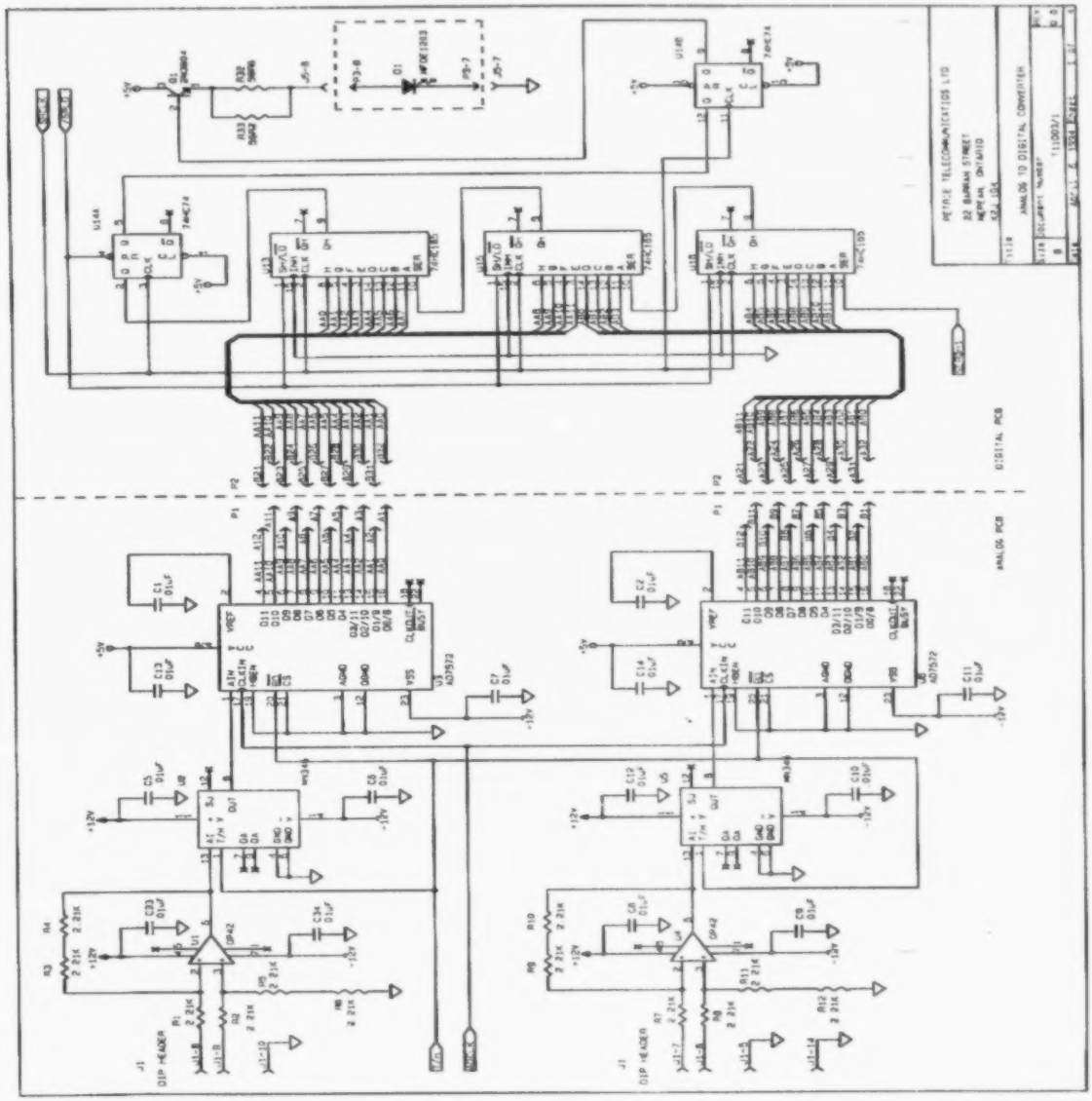
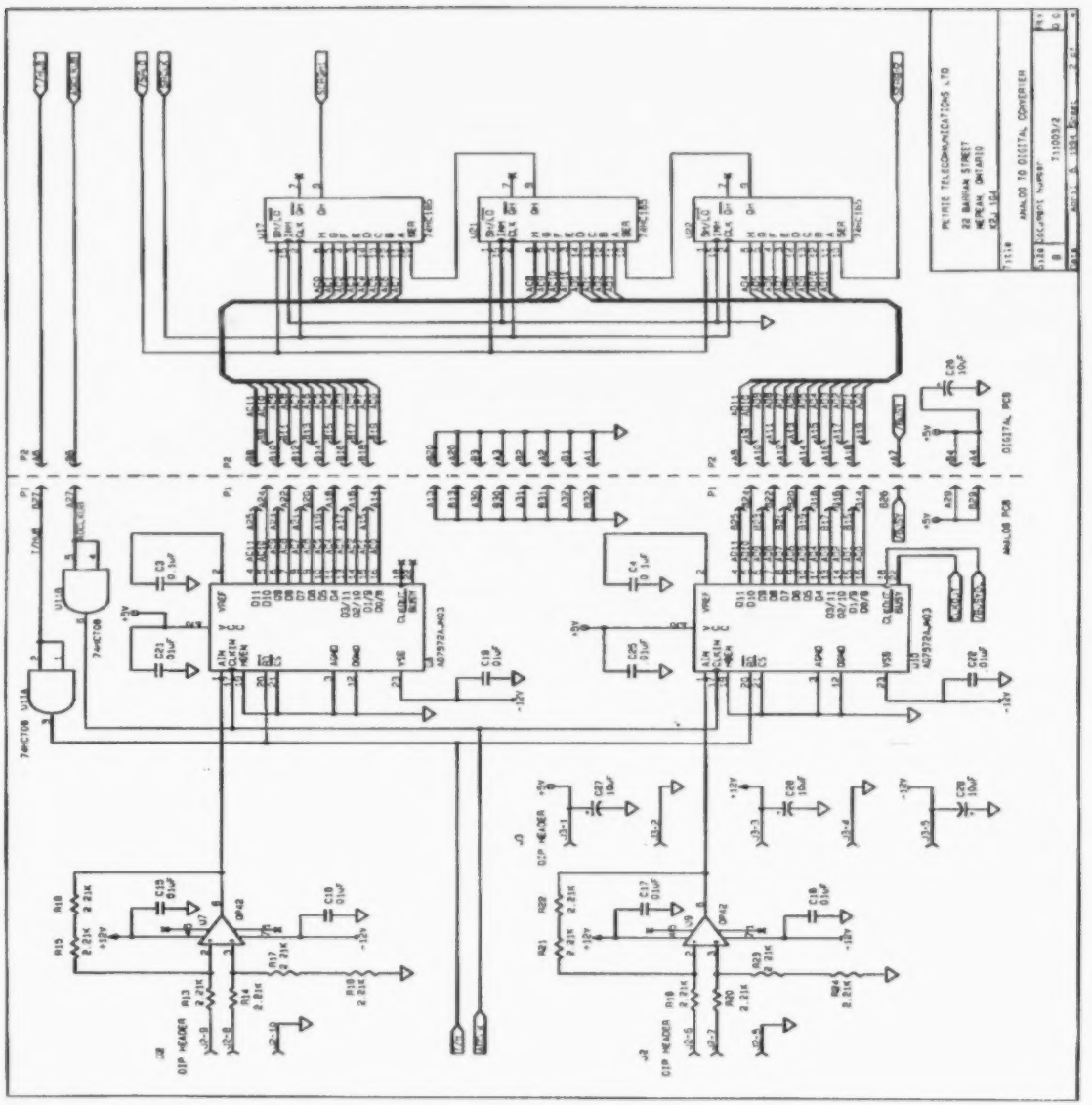
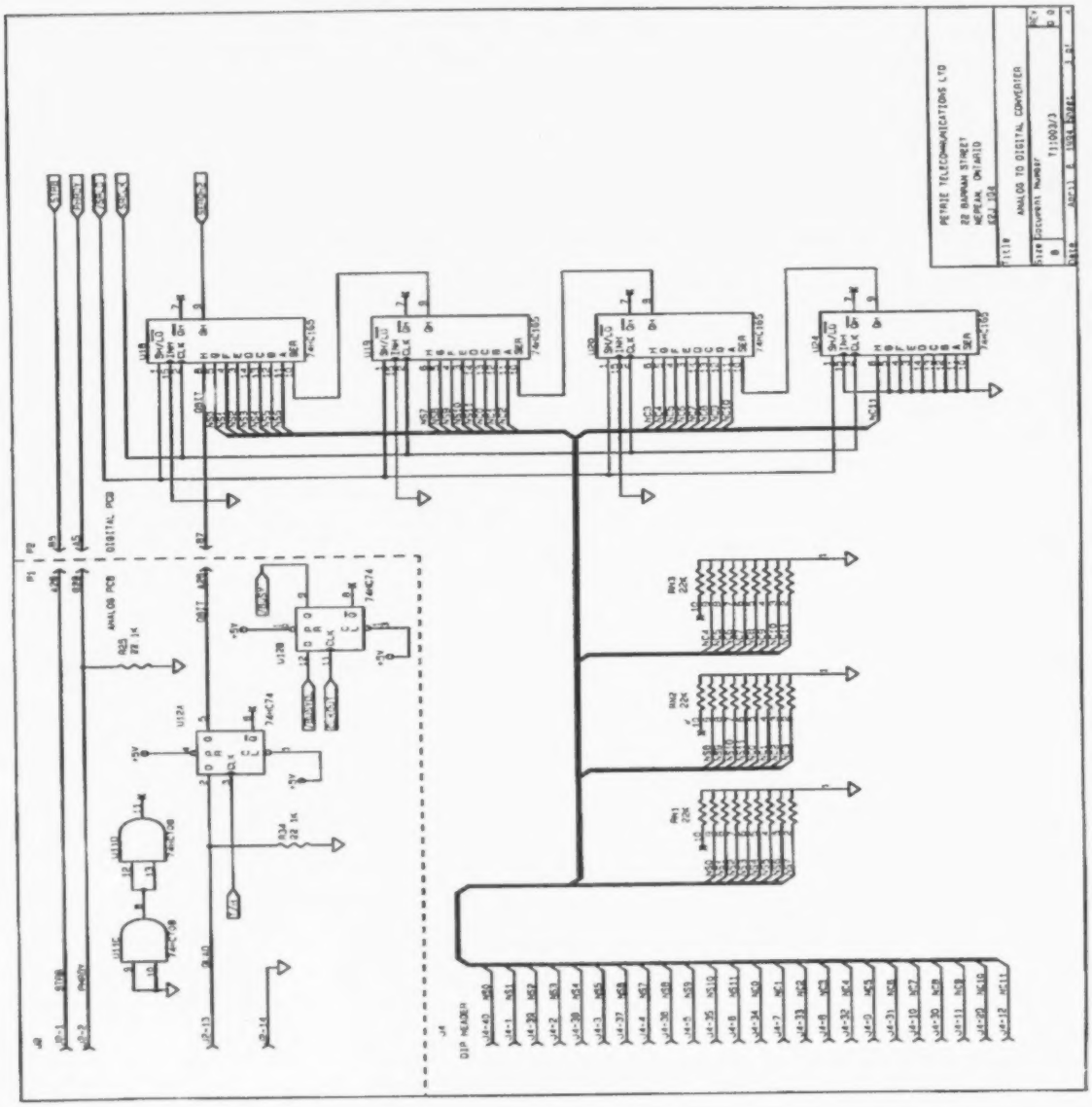
VCC2
NOTE
MECL "0" = -1.75V, "1" = -0.8V






PETRIE TELECOMMUNICATIONS LTD
22 BARRAN STREET
NEPEAN, ONTARIO
K2E 7S6
ANALOG TO DIGITAL CONVERTER
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ANALOG PCB
DIP HEADER
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22K
22 1K

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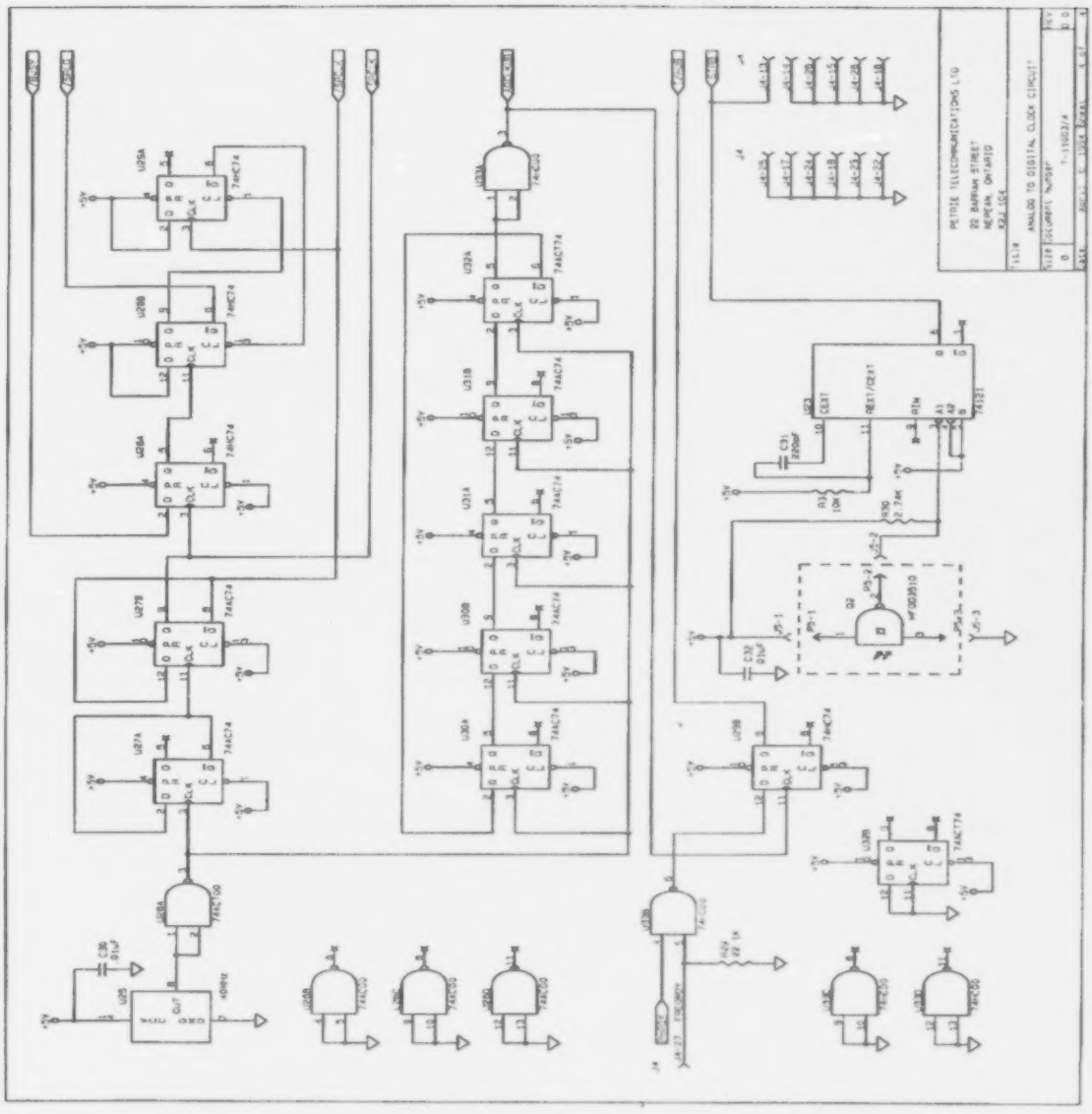

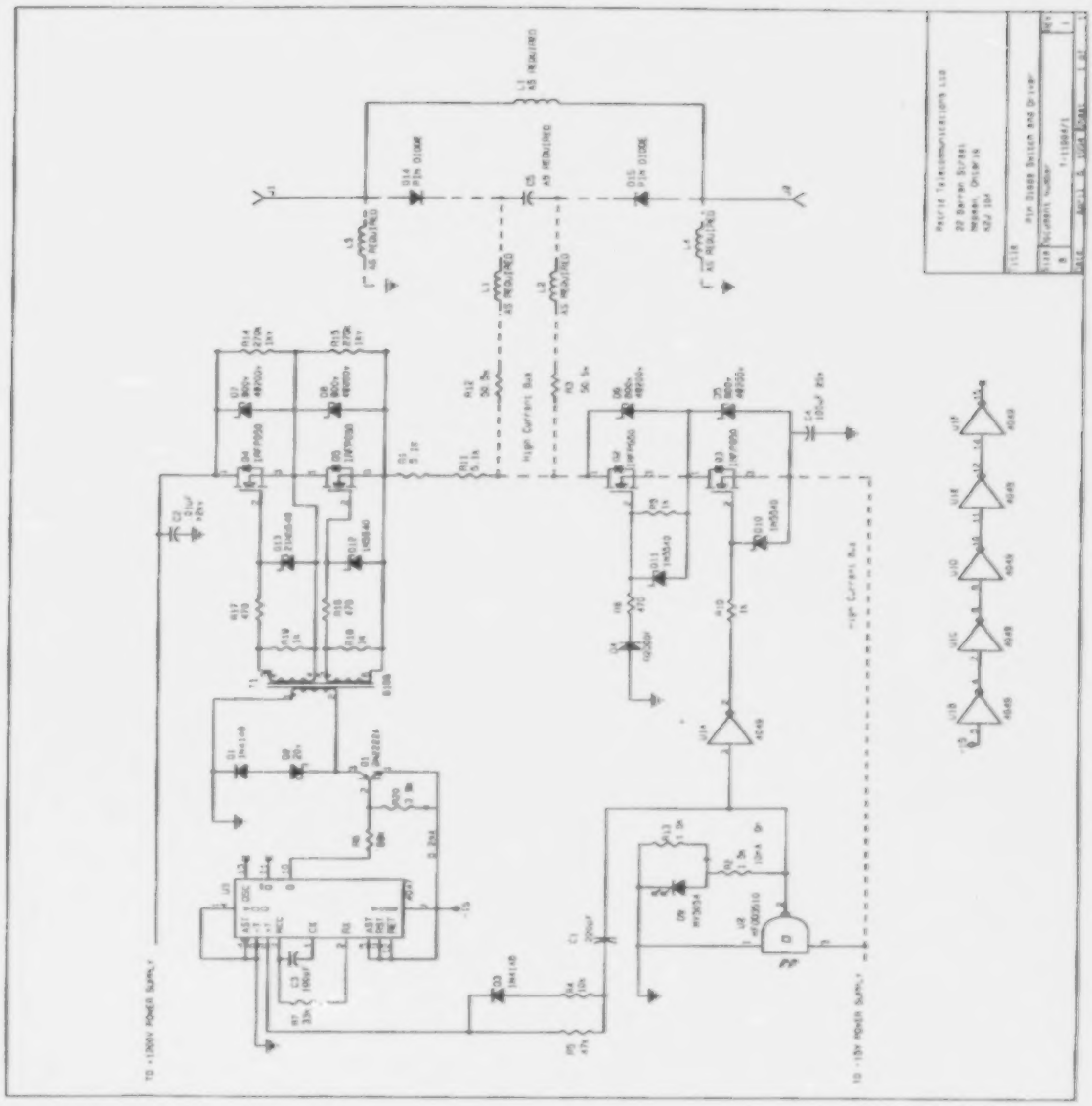

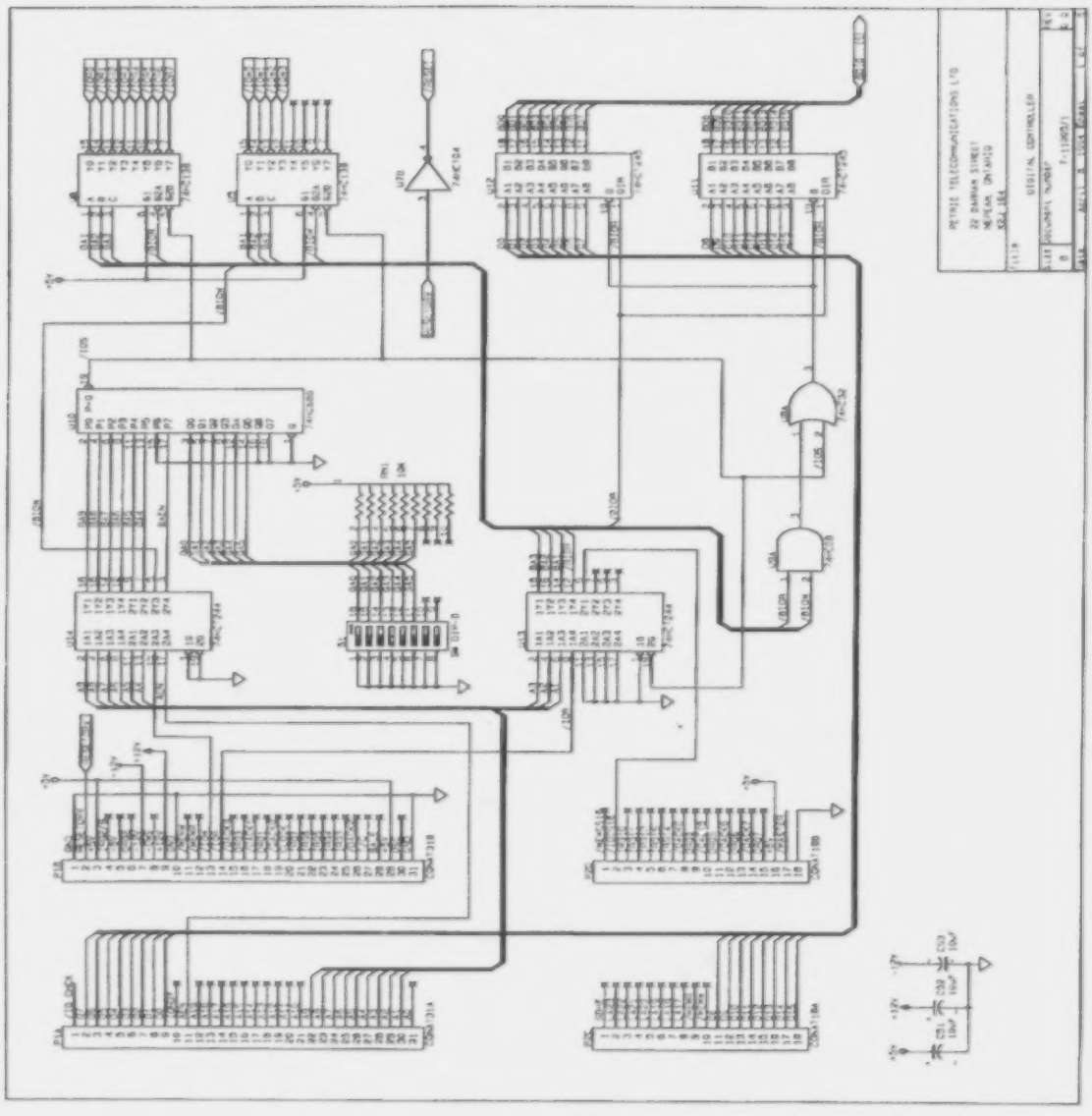

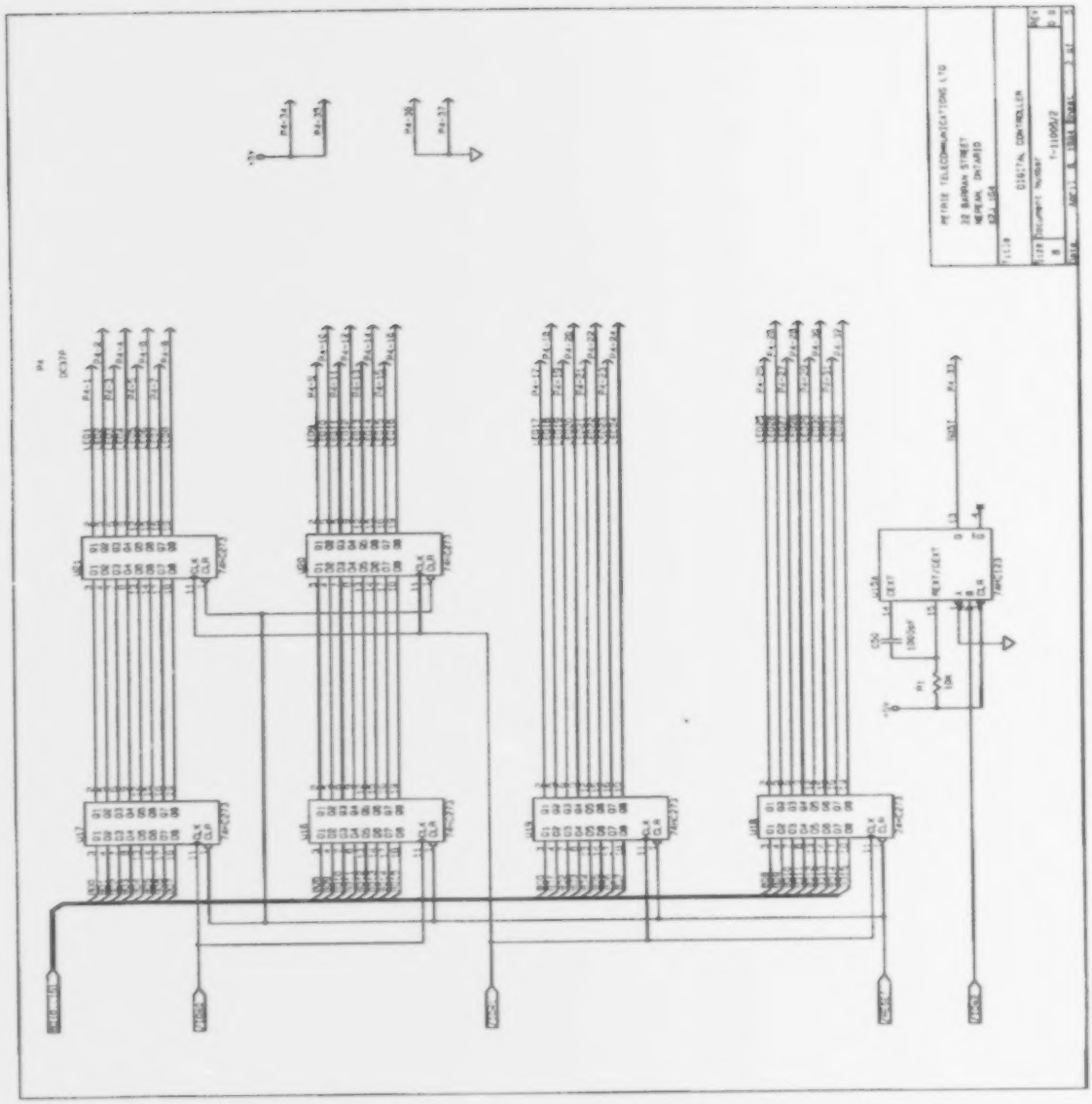

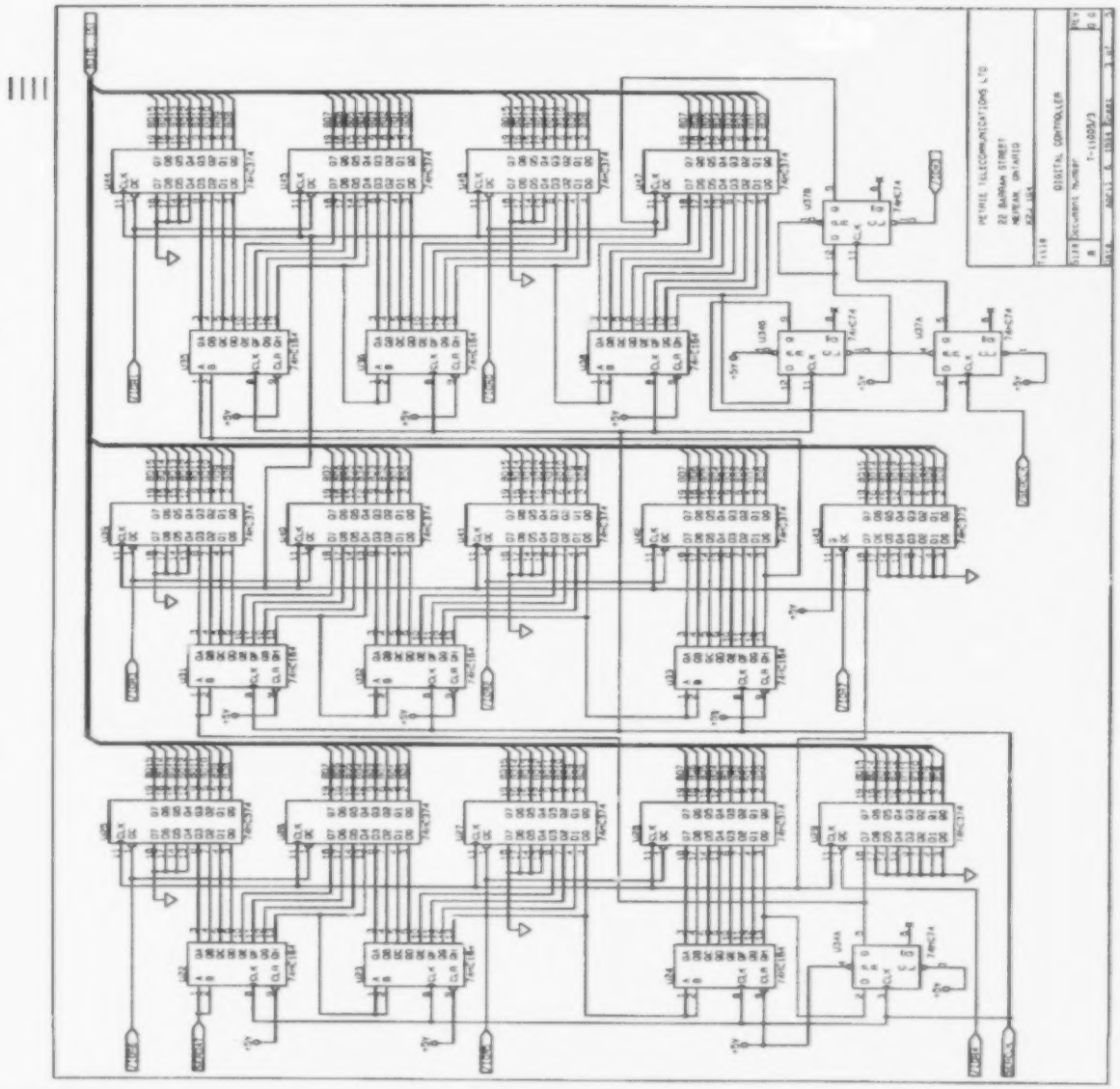

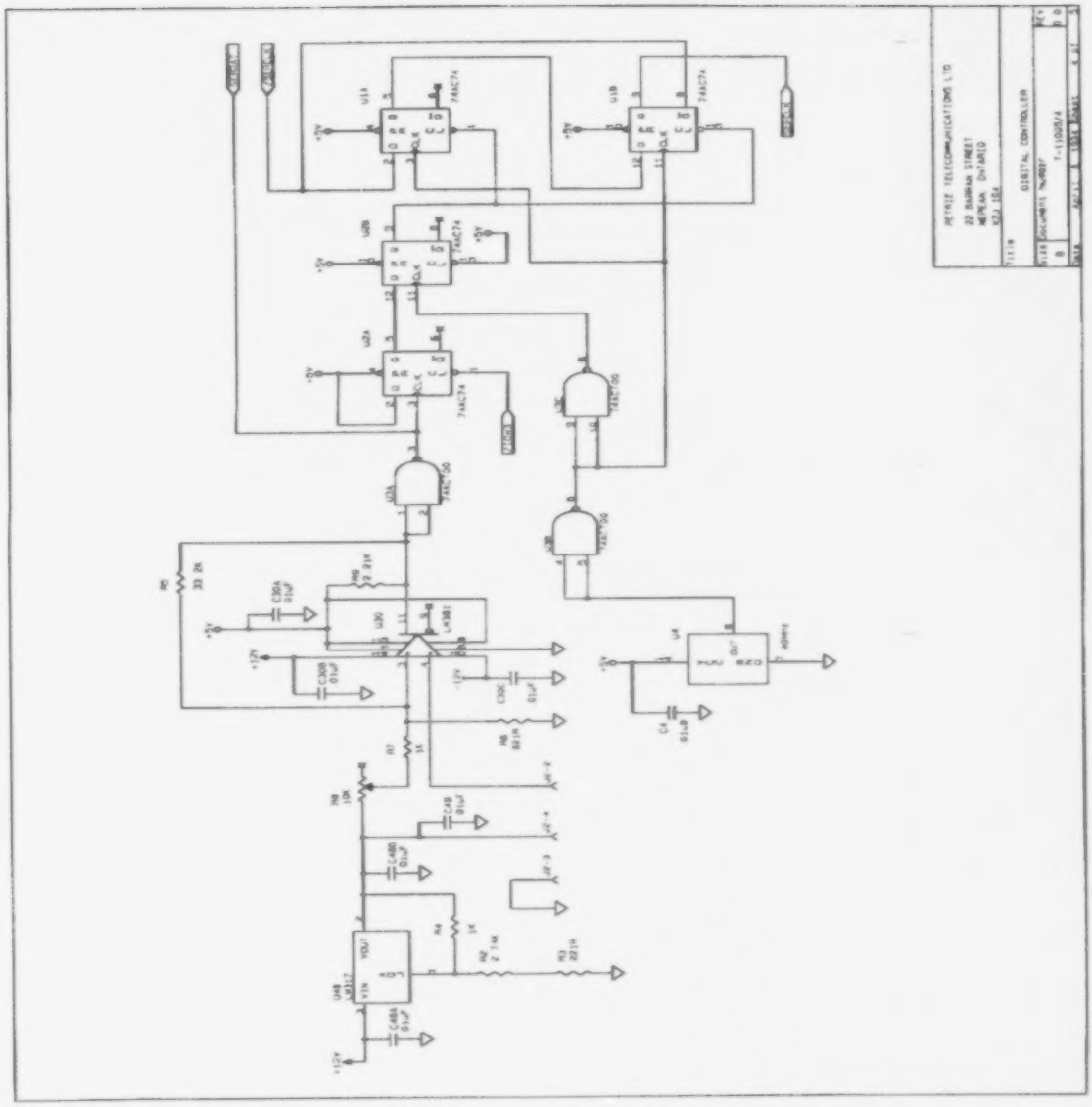
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74AC10
LM301
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+2.3
ADC+
ADC-

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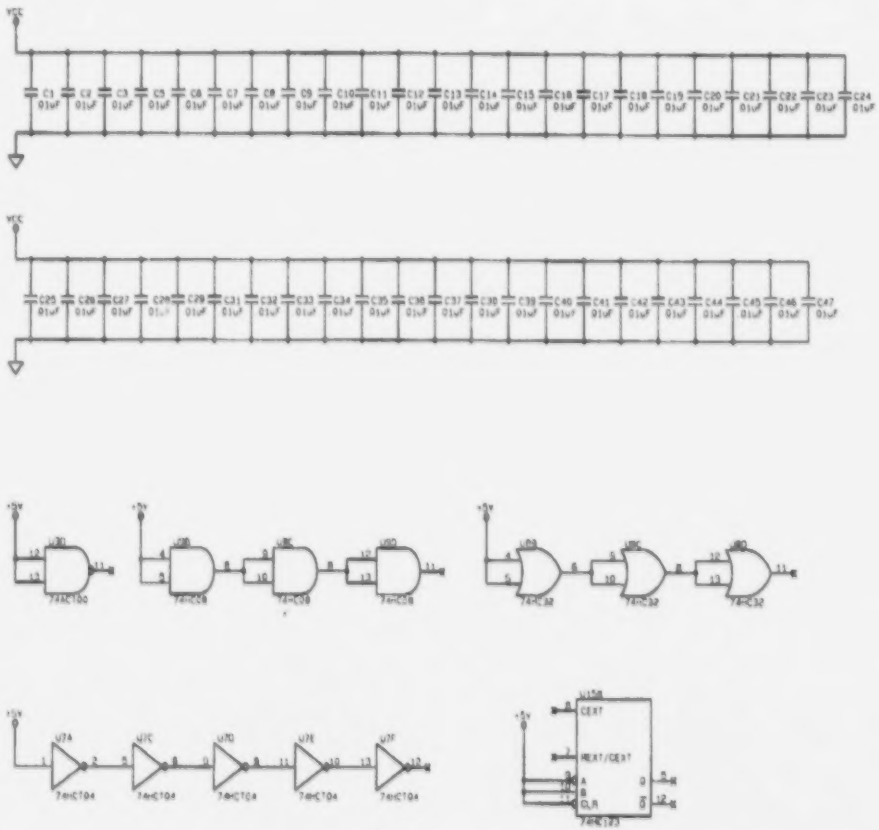


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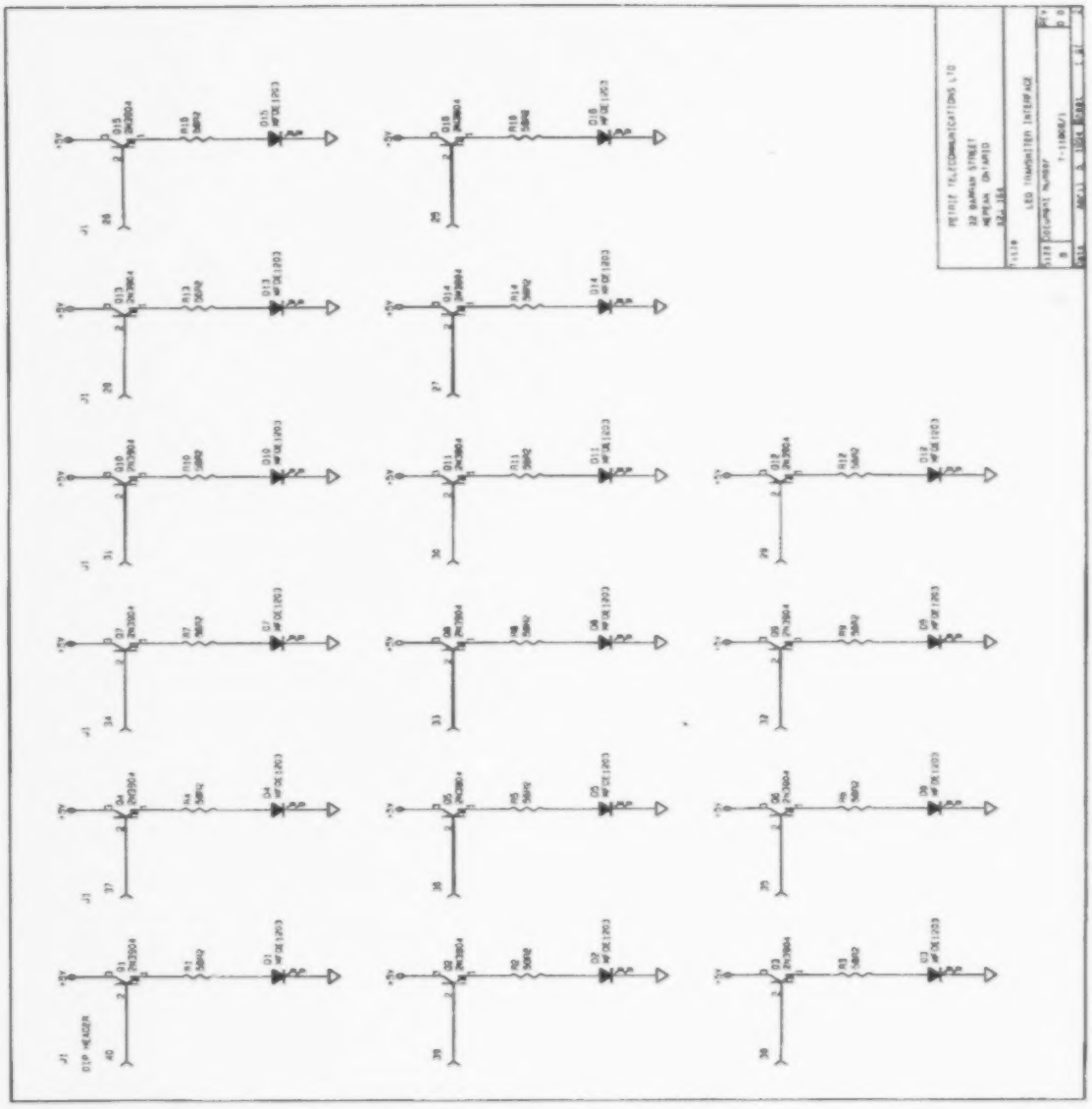

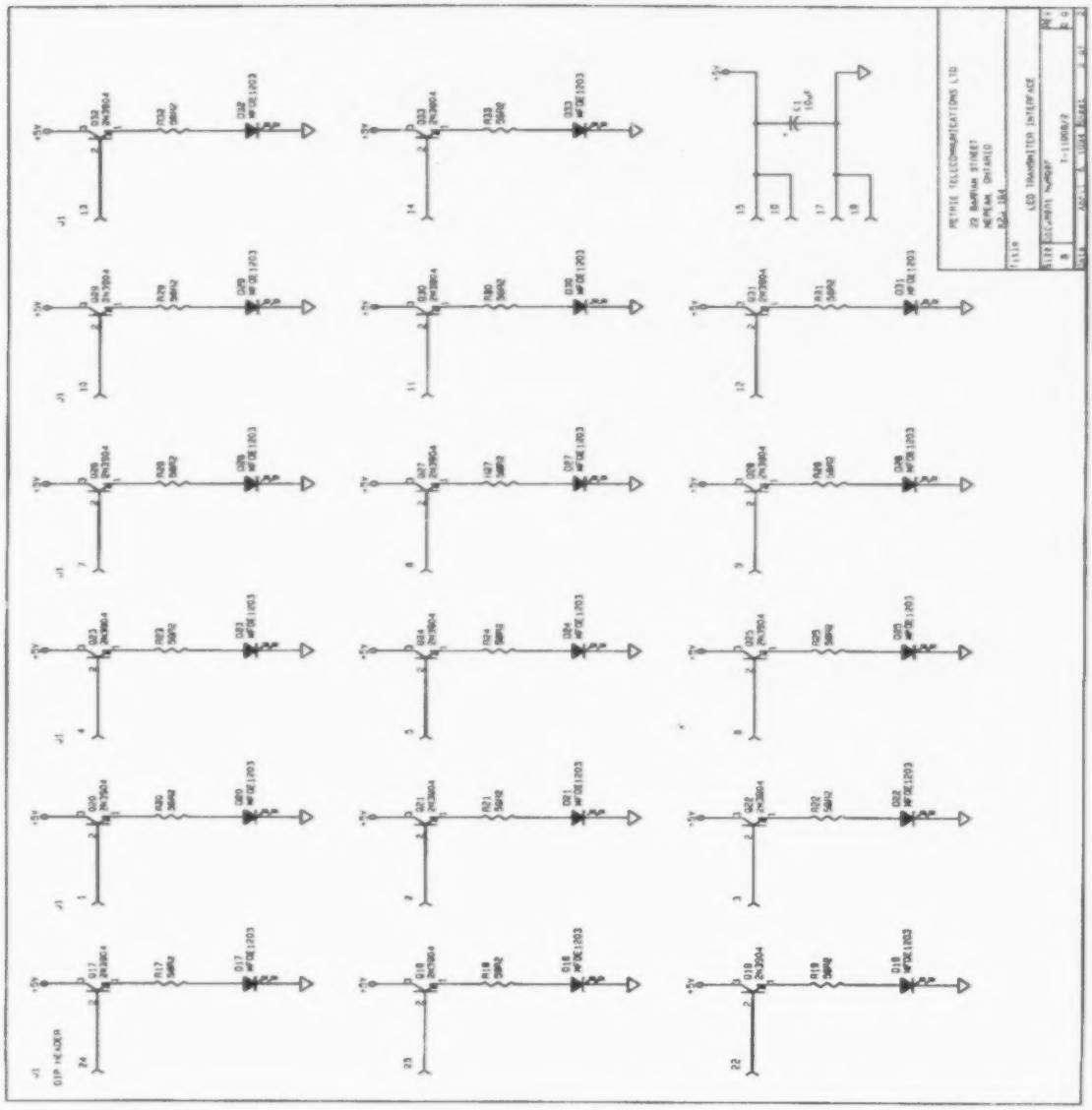
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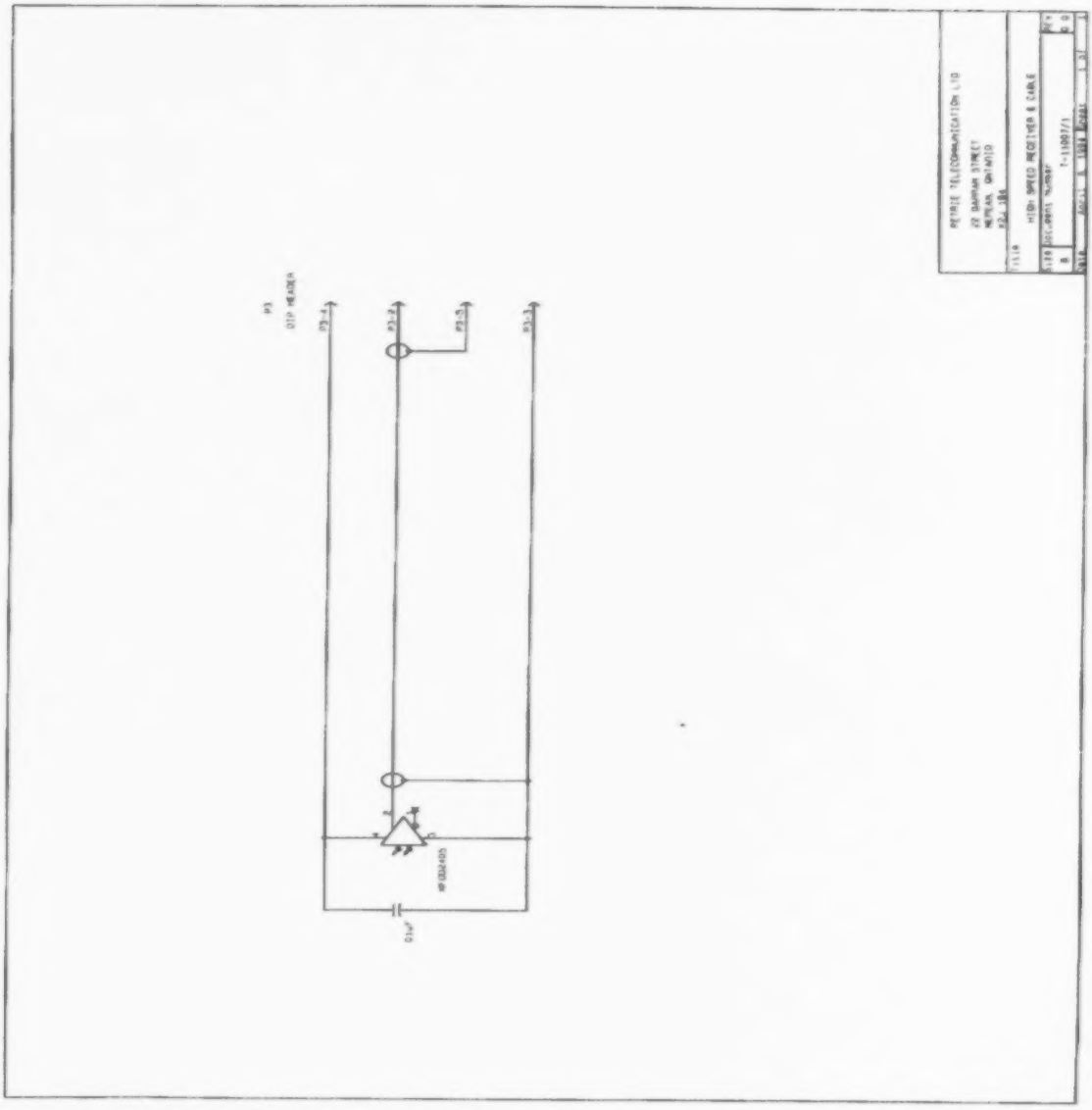
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DIP HEADER
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P3-2
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# APPENDIX A

## LIST OF SUBCONTRACTORS

T. Daniels
Daniels Electronic Ltd
43 Erie Street,
Victoria, B.C. V8V 1P8
Phone: 604 382-8268
Fax; 604 382-6139

J. Strickland
Diversitel Communications
8-21 Concourse Gate
Nepean, Ontario K2E 7S4
Phone: 613 727-0083
Fax; 613 272-5433

Richard Bonnycastle
Electronic Engineering Ltd
942 Arkell Street
Ottawa, Ontario K2B 5R3
Phone: 613 596-4665

K. Smith
Routes Inc.
Suite 202
329 March Road
Kanata, Ont. K2K 2E1
Phone: 613 592-0748
Fax; 613 592-6553

## APPENDIX B

TUNER LOSS & VSWR FOR ANTENNA WITH
RESISTANCE = 5, 50 and 1000 OHMS
REACTANCE = 500, 250, 0, -250, and -500 OHMS

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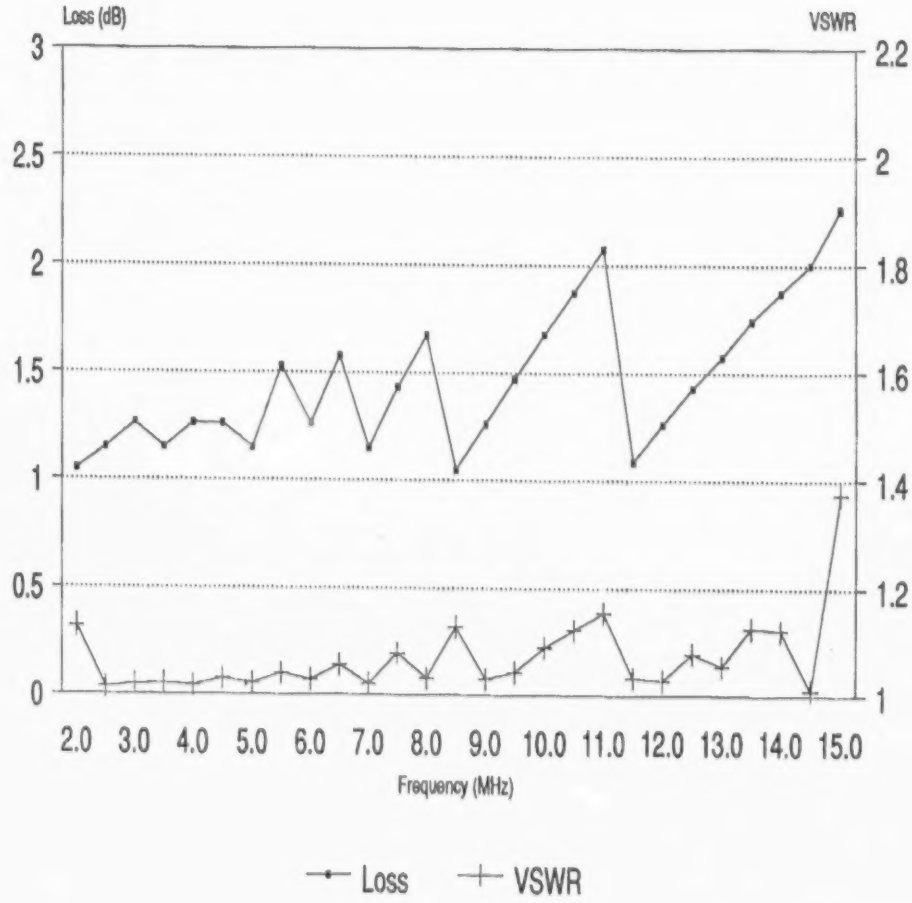
# Tuner Loss and VSWR

Resistance = 5 ohms
Reactance = 500 ohms



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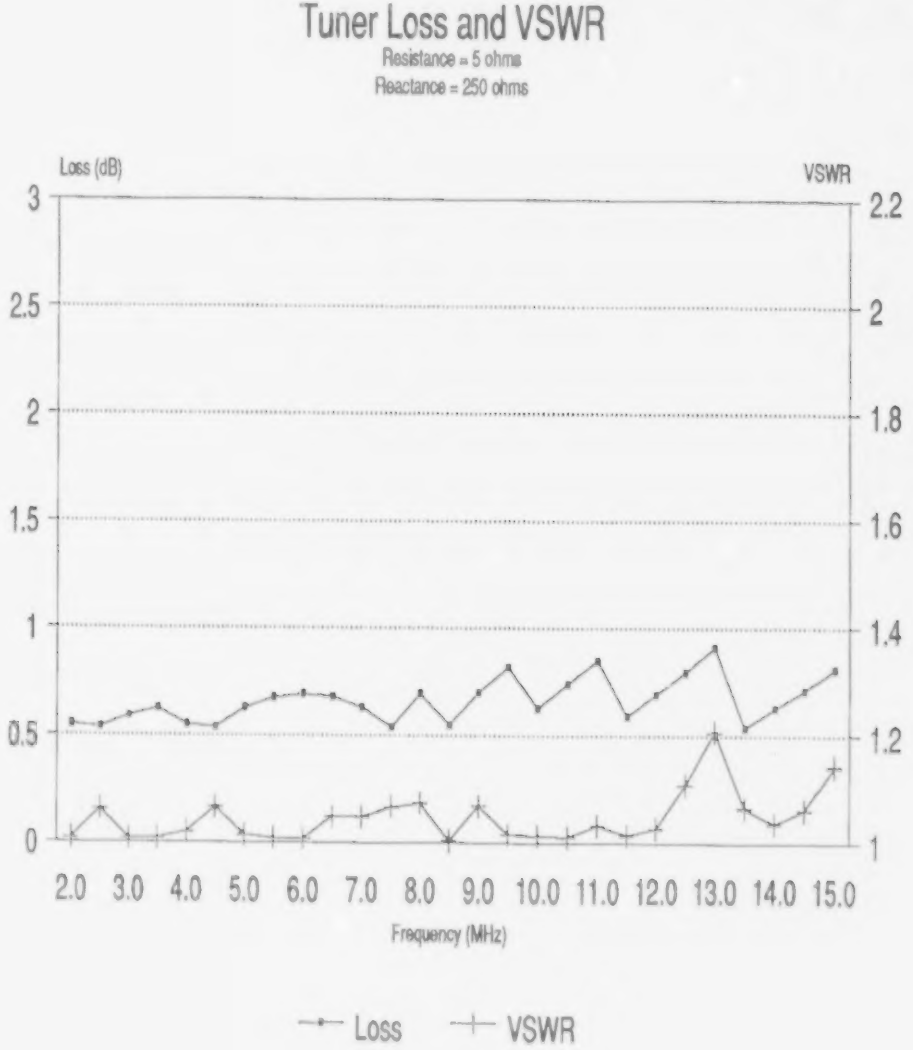

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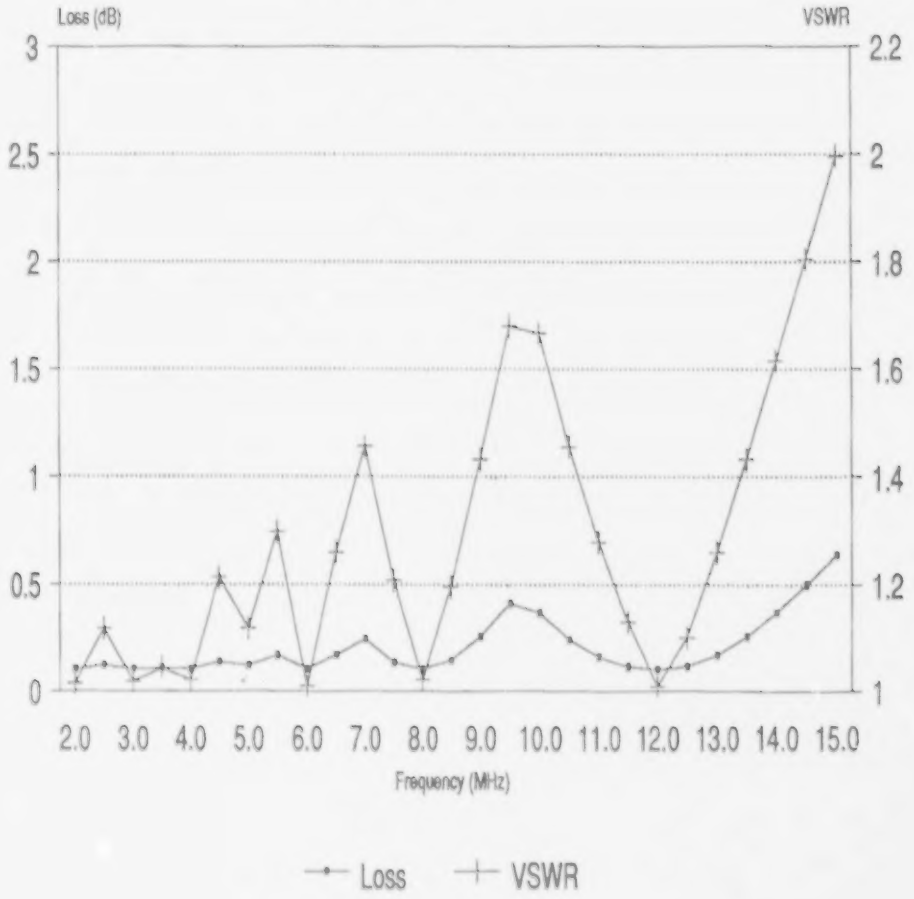
# Tuner Loss and VSWR

Resistance = 5 ohms
Reactance = 0 ohms



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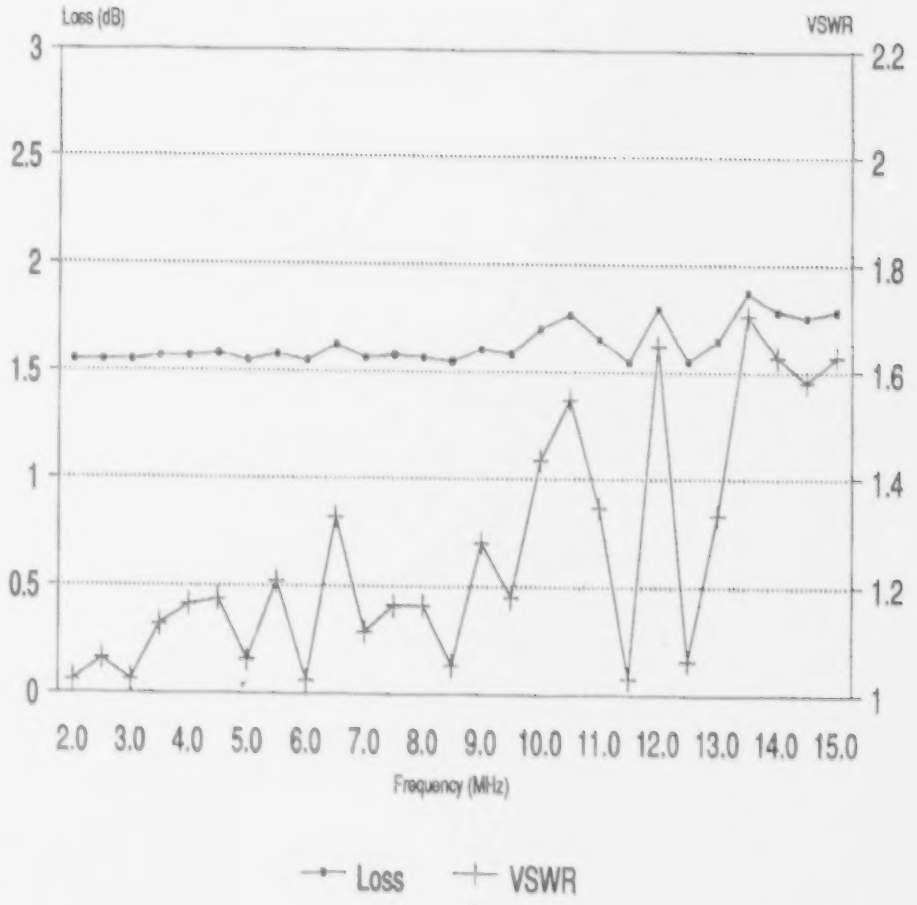
## Tuner Loss and VSWR

Resistance = 5 ohms
Reactance = -250 ohms

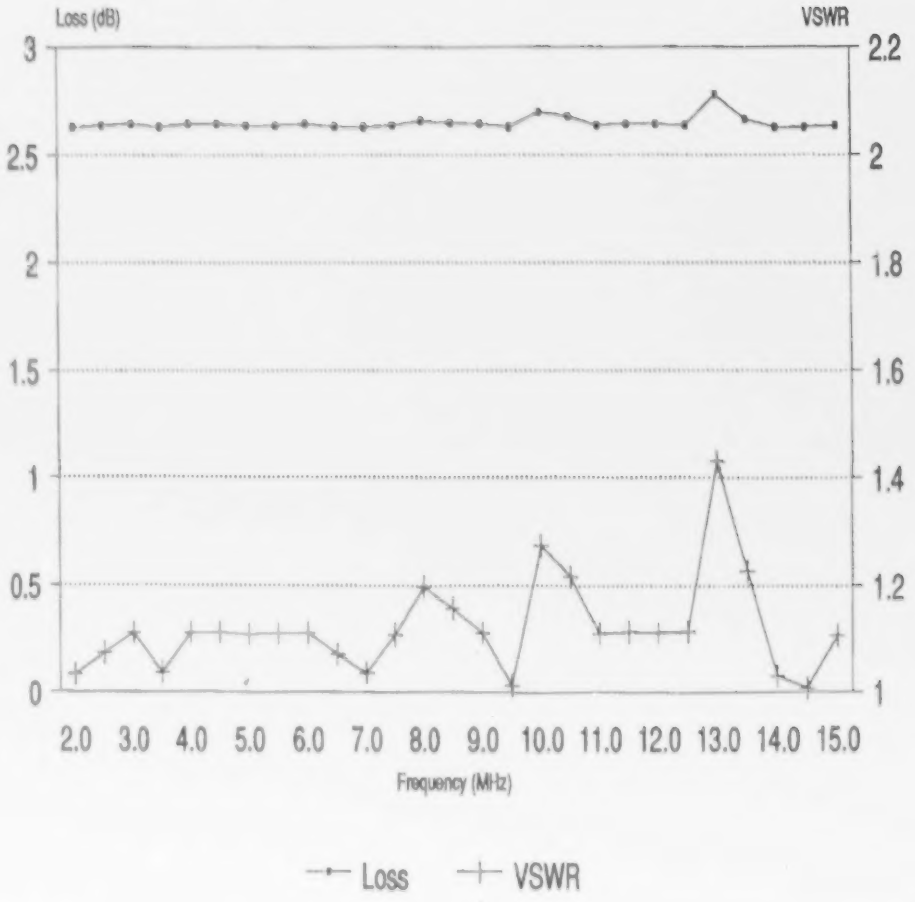


P149048.PDF [Page 73 of 120]

# Tuner Loss and VSWR

Resistance = 5 ohms

Reactance = -500 ohms



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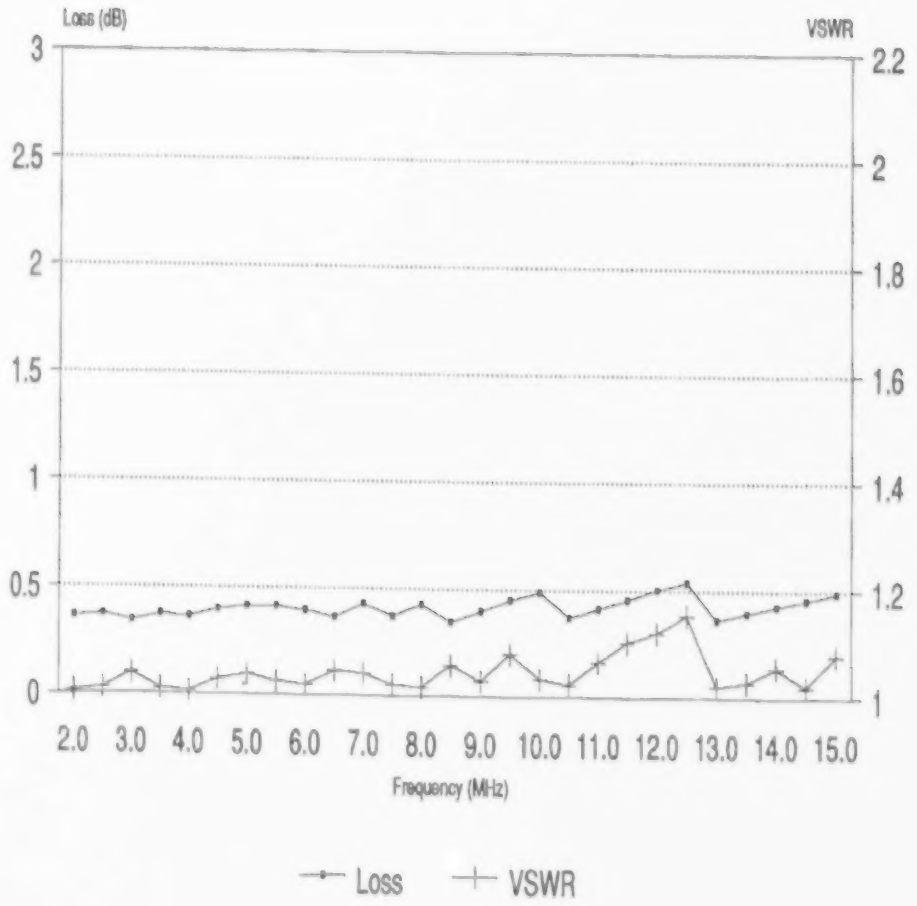
## Tuner Loss and VSWR

Resistance = 50 ohms
Reactance = 500 ohms



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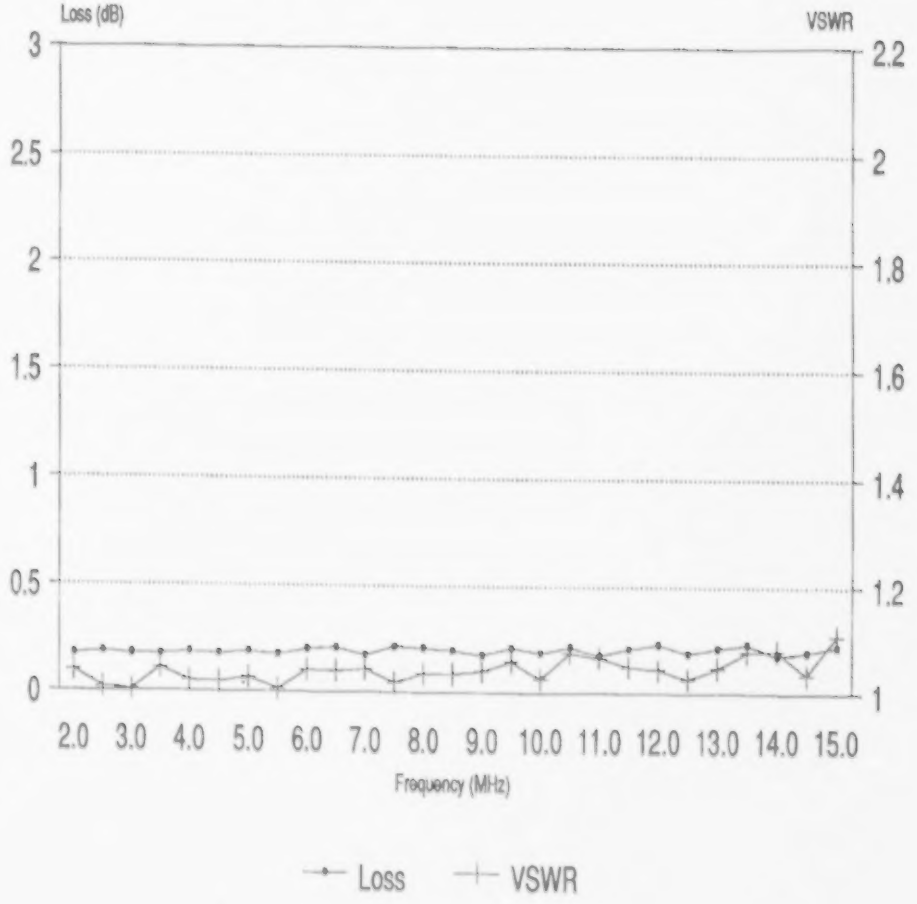
# Tuner Loss and VSWR

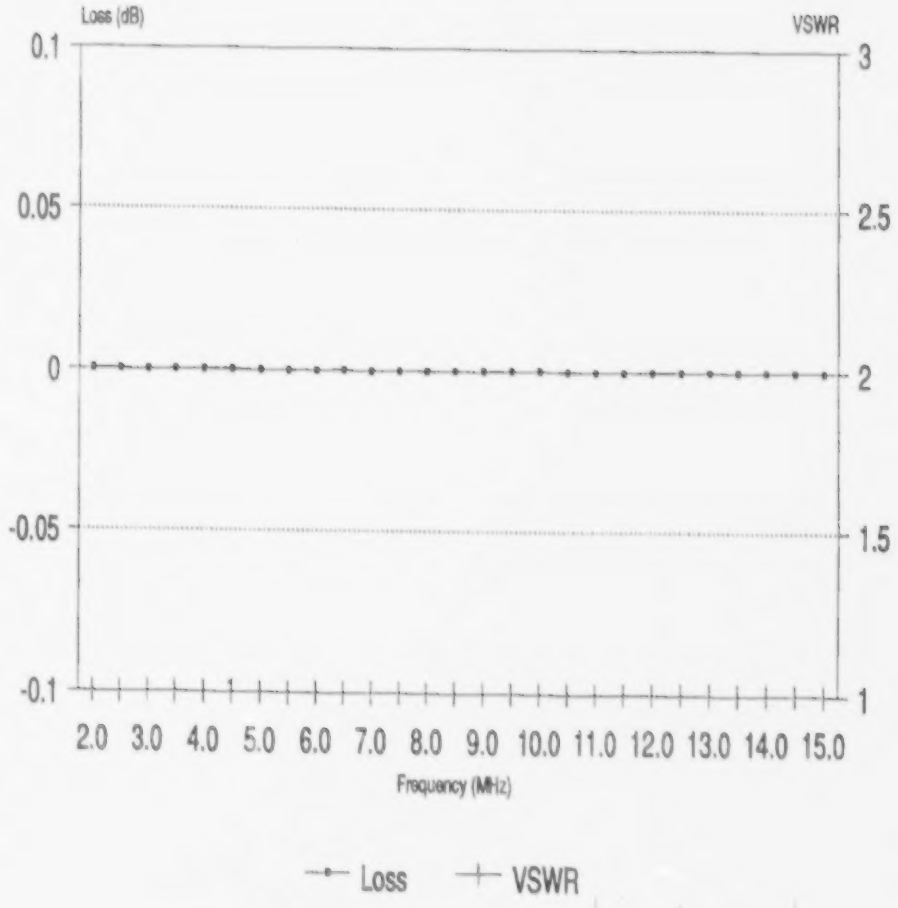
Resistance = 50 ohms
Reactance = 250 ohms



P149048.PDF [Page: 76 of 120]

# Tuner Loss and VSWR

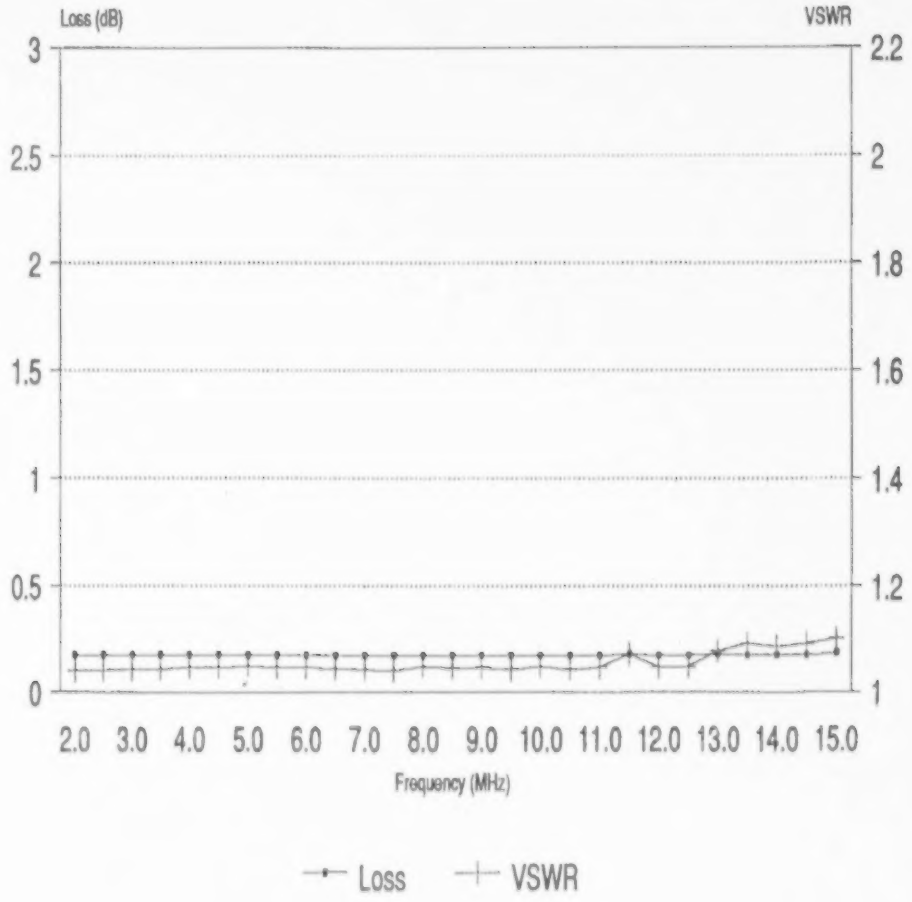
Resistance = 50 ohms
Reactance = 0 ohms



P149048.PDF [Page: 77 of 120]

# Tuner Loss and VSWR

Resistance = 50 ohms
Reactance = -250 ohms



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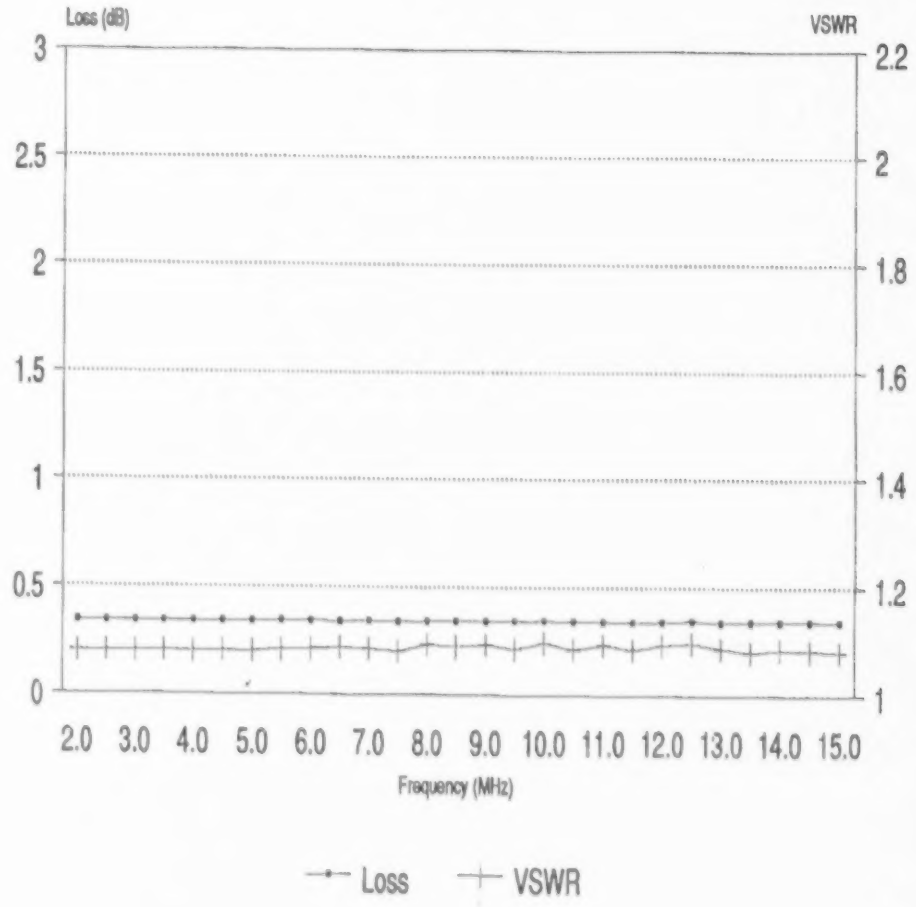
# Tuner Loss and VSWR

Resistance = 50 ohms
Reactance = -500 ohms



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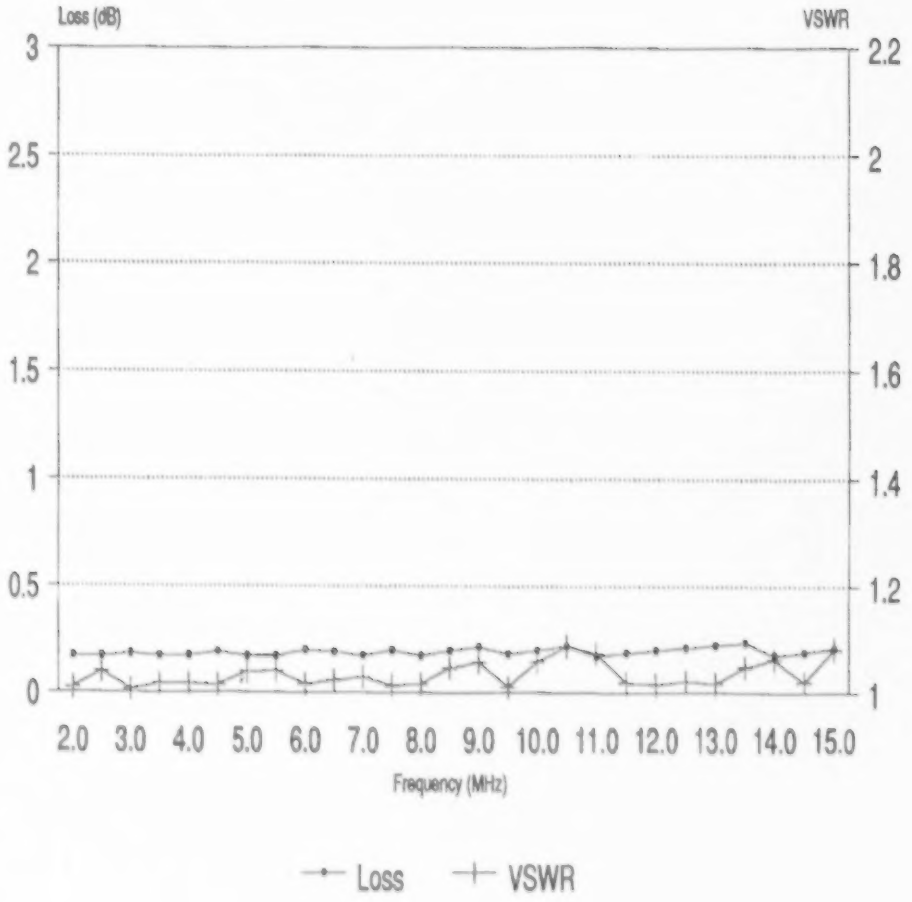
# Tuner Loss and VSWR

Resistance = 1000 ohms
Reactance = 500 ohms



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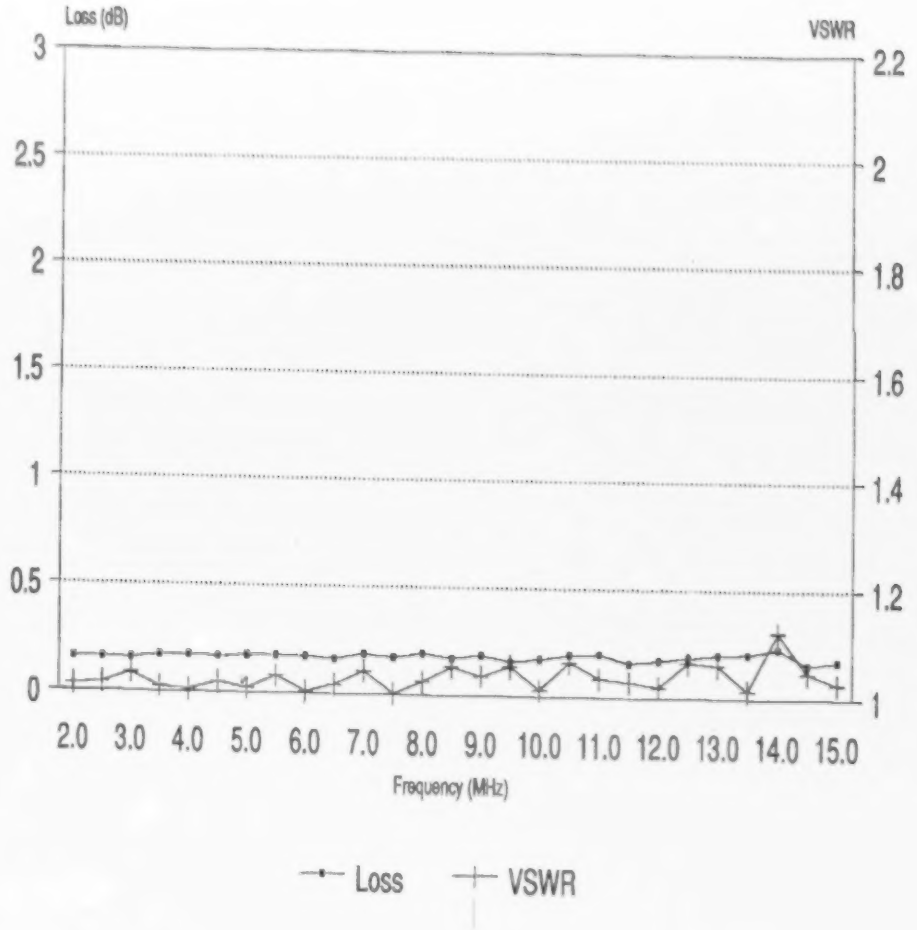
# Tuner Loss and VSWR

Resistance = 1000 ohms
Reactance = 250 ohms



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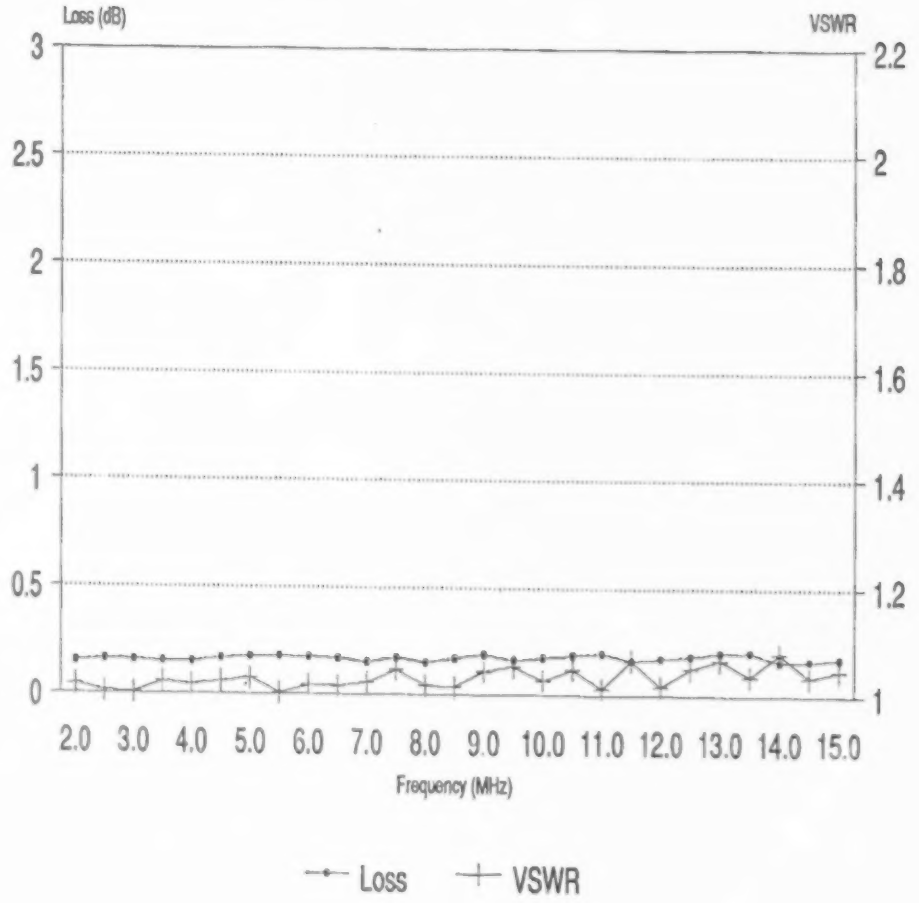

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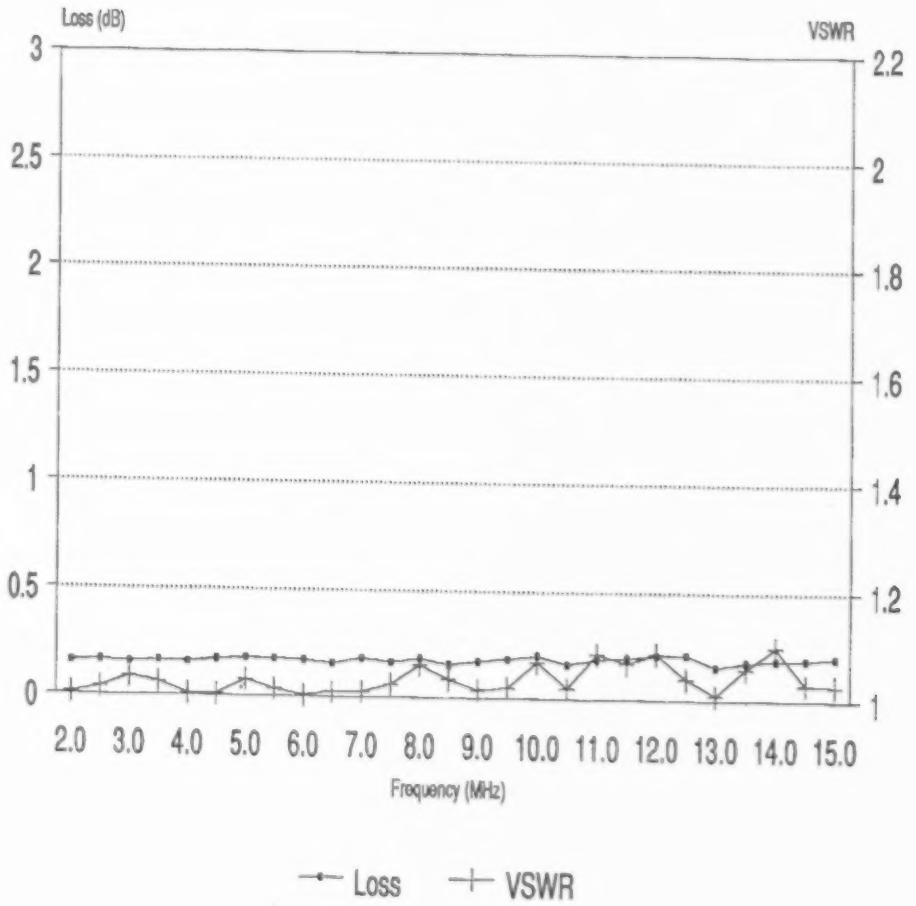
# Tuner Loss and VSWR

Resistance = 1000 ohms
Reactance = -250 ohms



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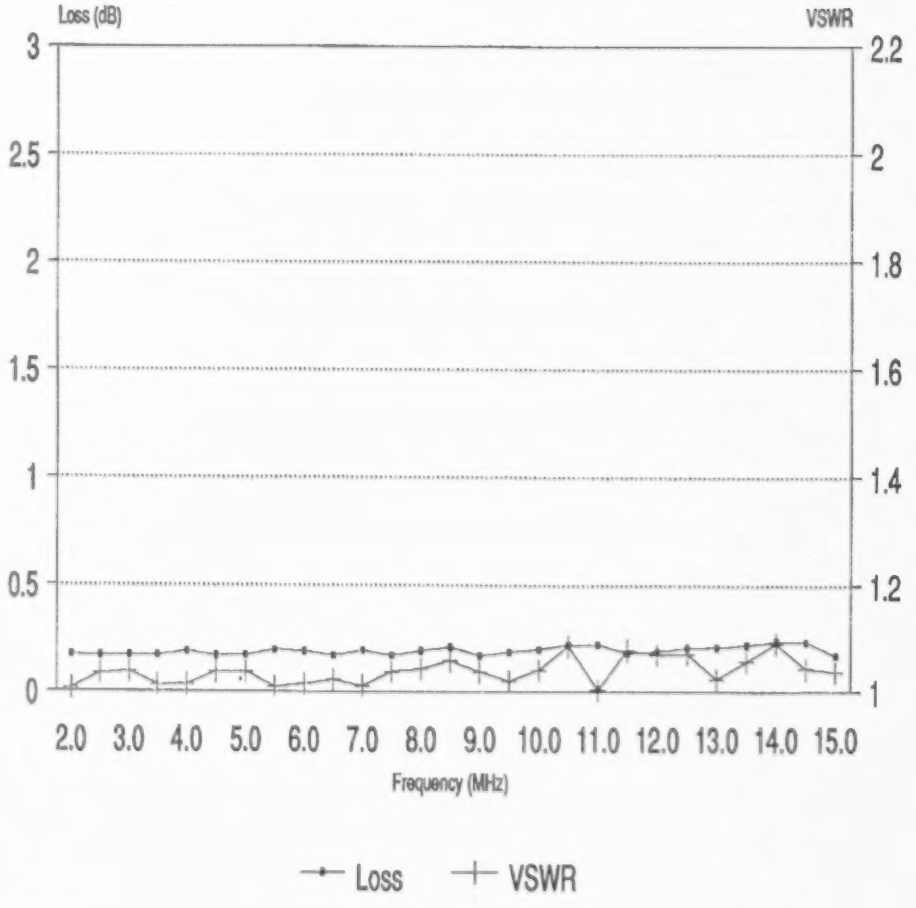
# Tuner Loss and VSWR

Resistance = 1000 ohms
Reactance = -500 ohms



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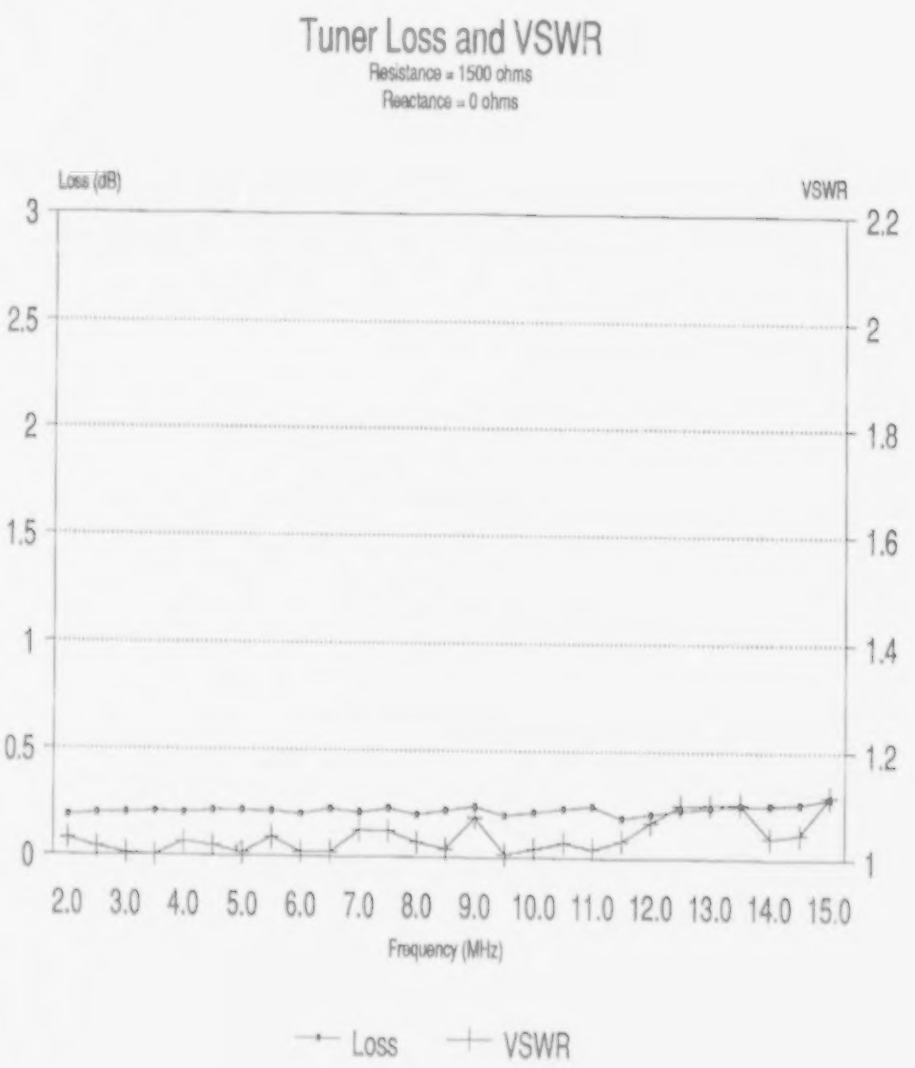

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# APPENDIX C

## VARIATION OF VSWR WITH CHANGES IN COMPONENT VALUES IN $\pi$-NETWORK

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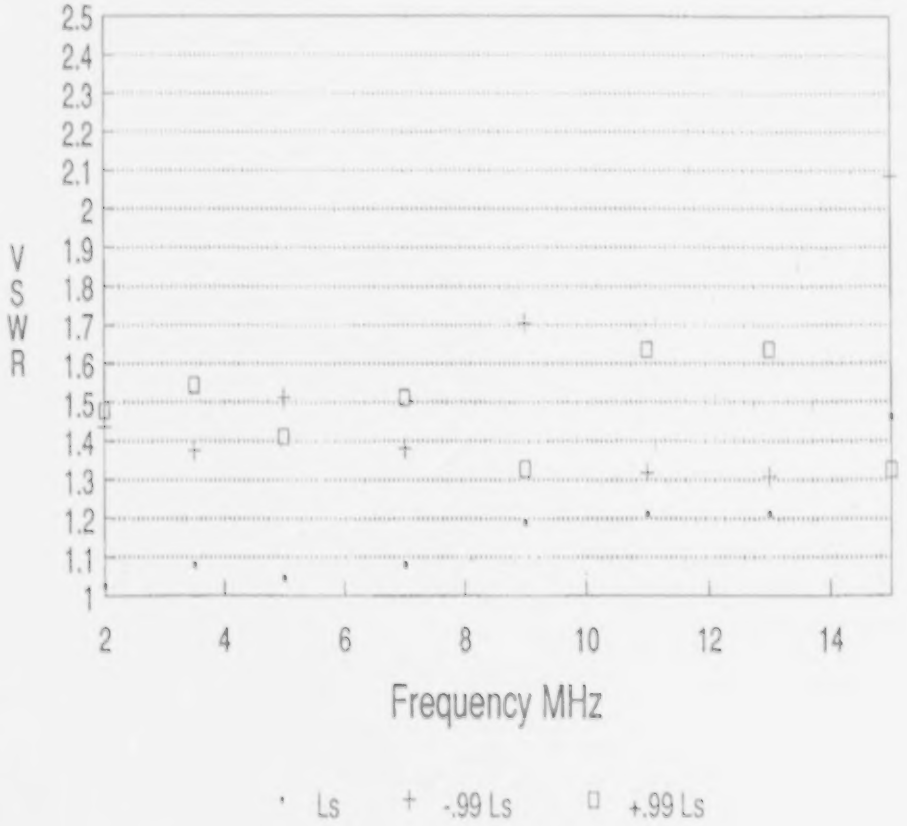
## Variation of VSWR with Ls

Ant. Reactance -250 ohms

Ant. Resistance 5 ohms, Q of Coil = 125



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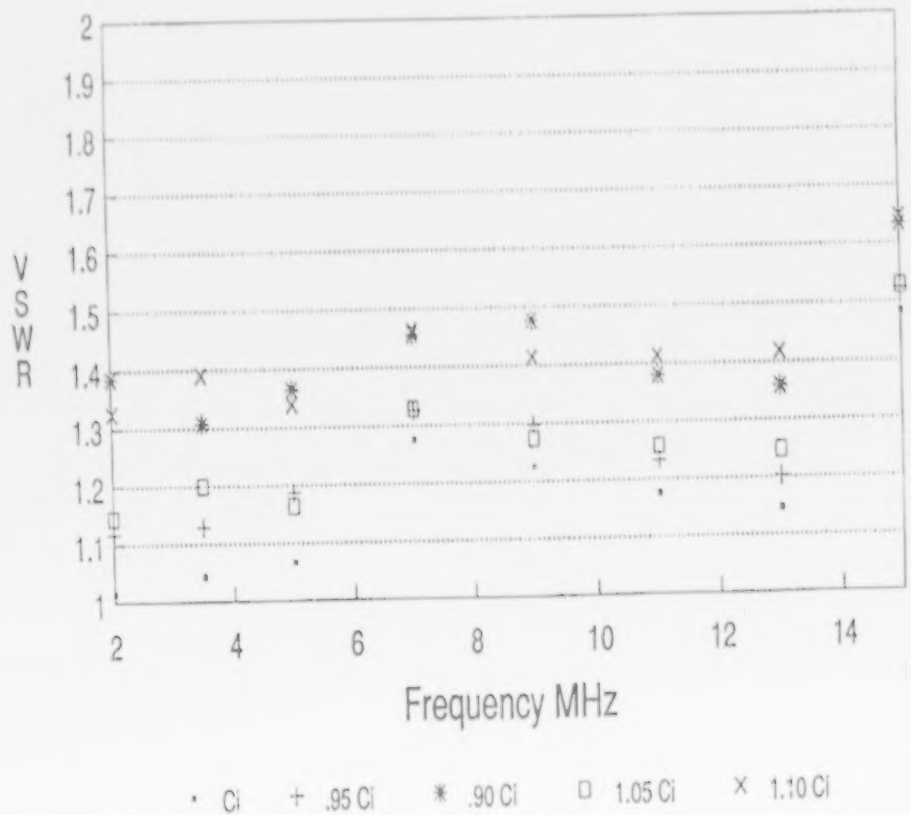

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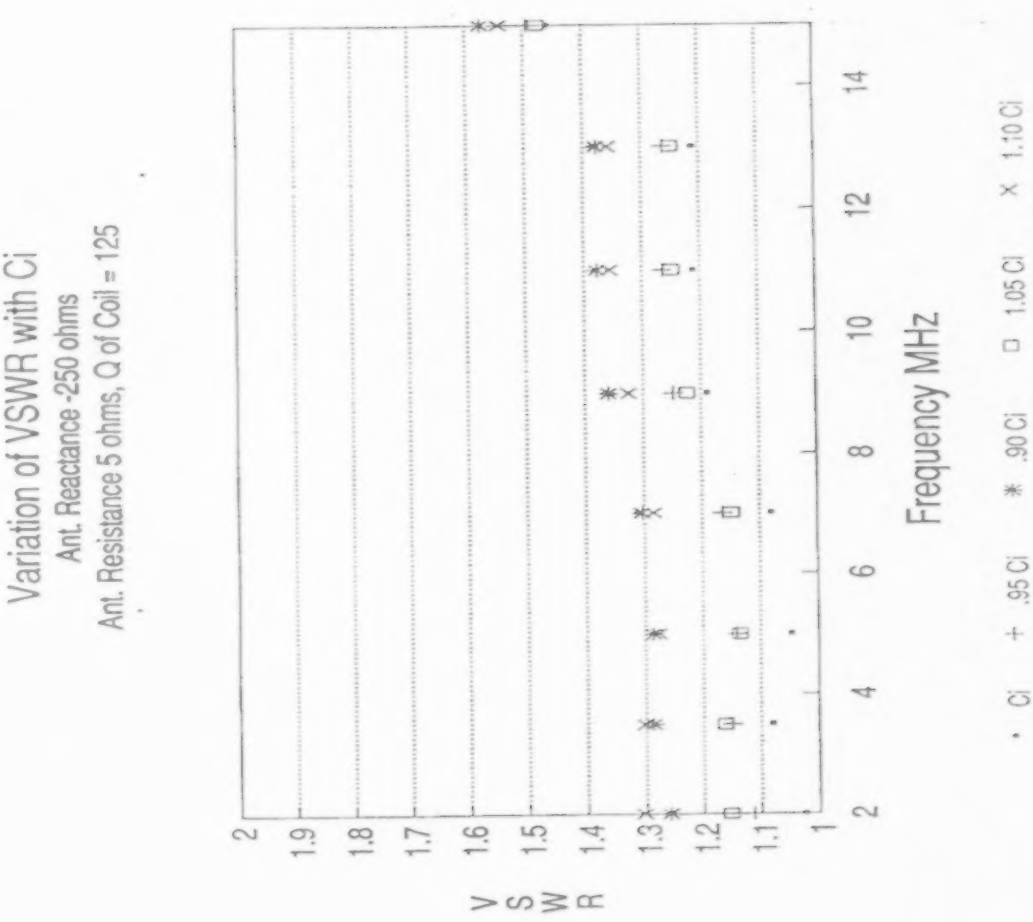

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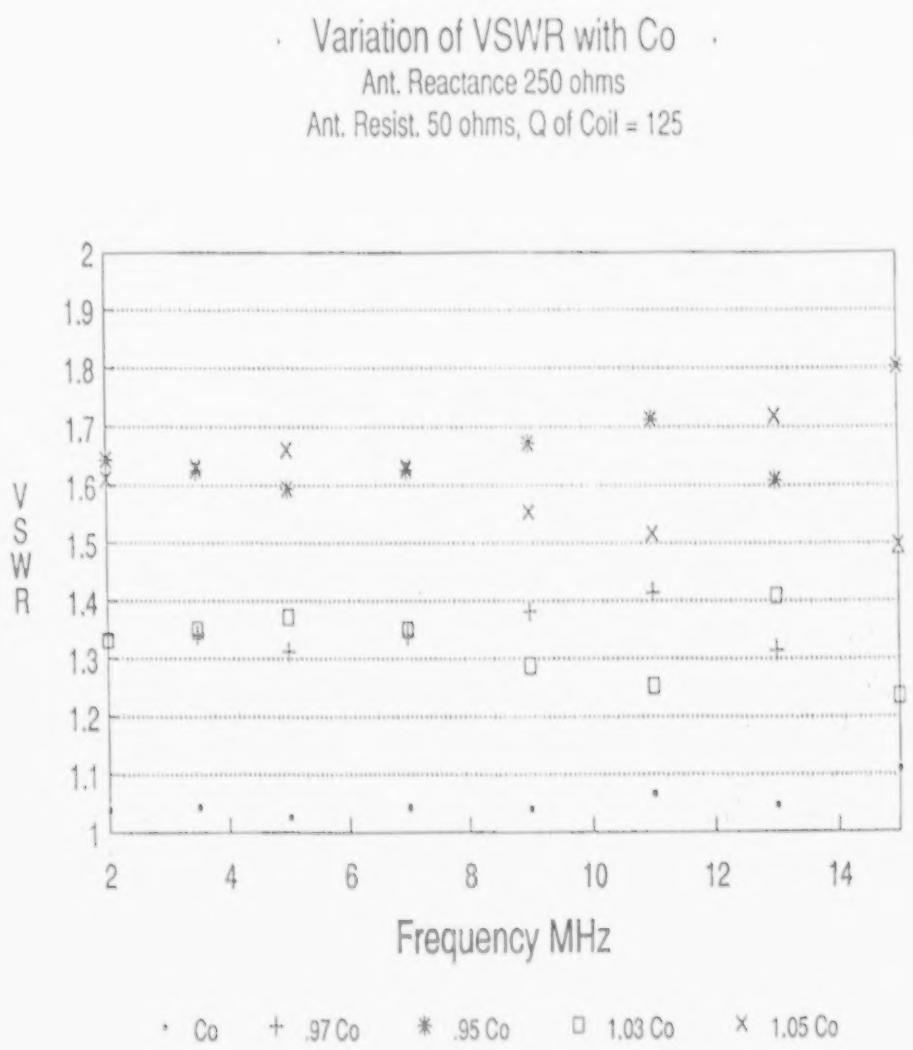

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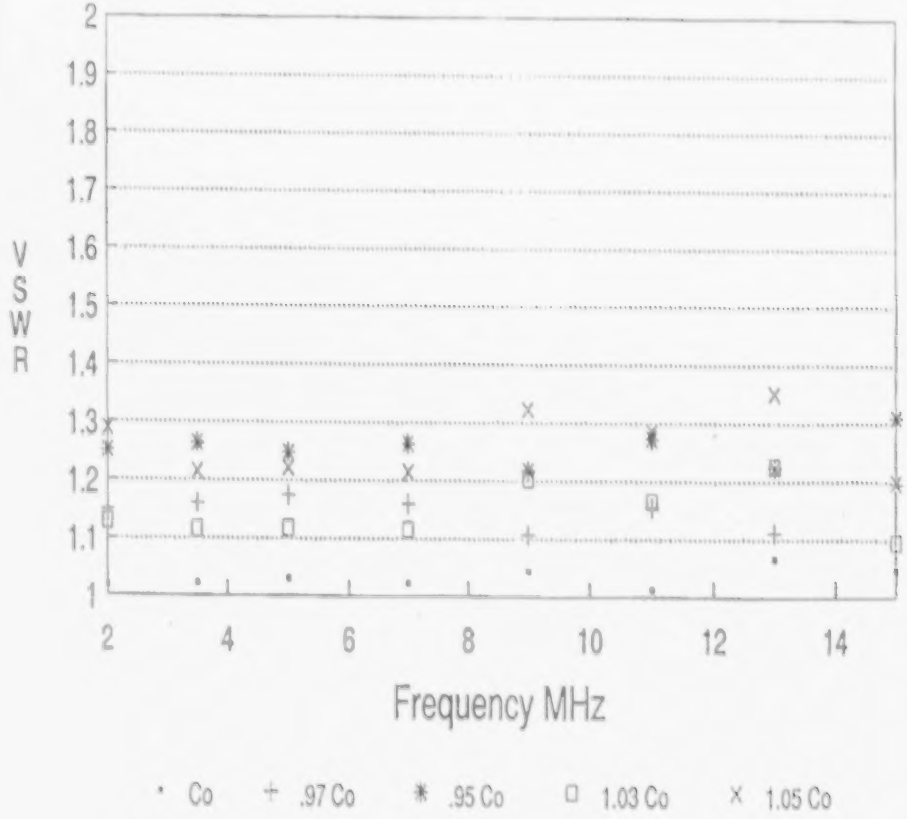
## Variation of VSWR with Co

Ant. Reactance 0 ohms

Ant. Resist. 1000 ohms, Q of Coil = 125



# APPENDIX D

## COMPUTATION OF INITIAL VALUES OF Ls, Ci, and Co
## FLOW CHART AND LISTING OF COMPUTER PROGRAM
## VSWR BASED ON THE INITIAL VALUES

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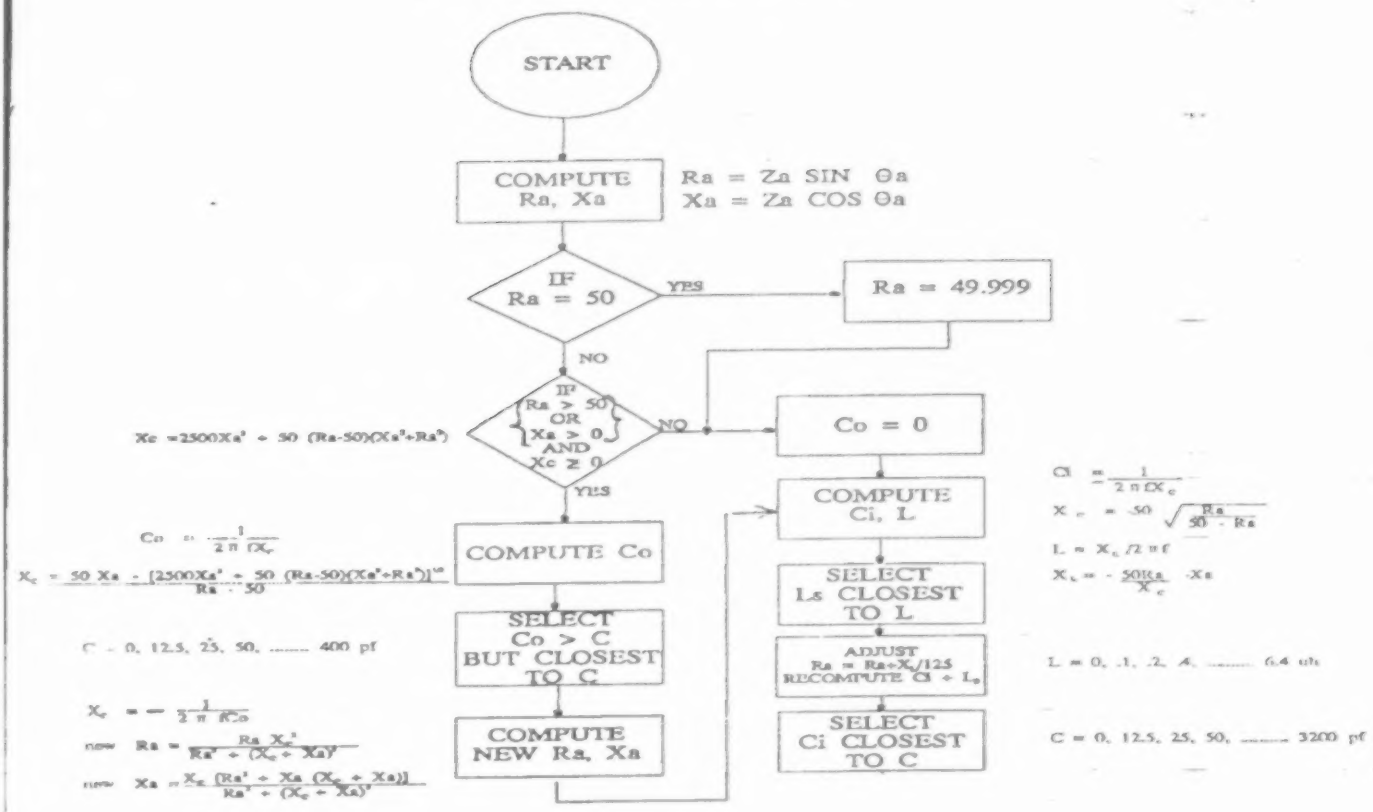
# CALCULATE INITIAL L & C


START
COMPUTE Ra, Xa
Ra = Za SIN θa
Xa = Za COS θa
IF Ra = 50
YES
Ra = 49.999
NO
IF Ra > 50 OR Xa > 0 AND Xc ≥ 0
NO
Co = 0
YES
COMPUTE Co
COMPUTE Ci, L
SELECT Co > C BUT CLOSEST TO C
SELECT Ls CLOSEST TO L
ADJUST Ra = Ra+Xc/125 RECOMPUTE Ci + Lo
COMPUTE NEW Ra, Xa
SELECT Ci CLOSEST TO C
Xc =2500Xa² ÷ 50 (Ra-50)(Xa²+Ra²)
Co = 1/2πfXc
Xc = 50 Xa - [2500Xa² ÷ 50 (Ra-50)(Xa²+Ra²)]^½ / Ra - 50
C = 0, 12.5, 25, 50, ..... 400 pf
Xc = 1/2πfCo
new Ra = Ra Xc² / Ra² ÷ (Xc ÷ Xa)²
new Xa = Xc [Ra² ÷ Xa (Xc ÷ Xa)] / Ra² ÷ (Xc ÷ Xa)²
Ci = 1/2πfXc
Xc = 50 √(Ra / 50 - Ra)
L = Xc /2πf
Xc = - 50Ra/Xc -Xa
L = 0, .1, .2, .4, ..... 6.4 uh
C = 0, 12.5, 25, 50, ..... 3200 pf

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```
#include <stdio.h>
#include <stdlib.h>
#include <math.h>

void  getlc (double, double, double, int, double*, double*, double*);

main()
{
  int     Q;
  double freq,  Xa, Ra, L, Co, Ci;

  /* Define Input Values */
  freq = 15.0e6;     /* Frequency in Hz */
  Xa = 0.0;          /* Measured value of antenna reactance */
  Ra = 5.0;          /* Measured value of antenna resistance */
  Q  = 125;          /* Measured Q of antenna */

  getlc (freq, Xa, Ra, Q, &L, &Ci, &Co);  /* Compute component values */
}


/* ------------------------------------------------------------------------ */

double ind_inc  =     0.1e-06;     /* Incremental steps of inductance  */
double ind_max  =   200.0e-06;     /* Maximum inductance               */
double cap_inc  =    12.5e-12;     /* Incremental steps of capacitance */
double cap1_max = 6387.5e-12;      /* Maximum input capacitance        */
double cap2_max = 4000.0e-12;      /* Maximum output capacitance       */

/* Input Parameters:
     freq:  Frequency in Hz
     Xa:    Antenna Reactance
     Ra:    Antenna Resistance
     Q:     Q of antenna

   Output Parameters:
     L:     Required inductance
     Ci:    Required input capacitor
     Co:    Required output capacitance
*/

void getlc (double freq, double Xa, double Ra, int Q, double *L, double *Ci, double *Co)
{
  int     i;
  double pif, xc, c, Xa2, Ra2, xcxa;
  char    string[12];

  pif = Pi2 * freq;

  Xa2 = Xa * Xa;
  Ra2 = Ra * Ra;
  if (Ra == 50.0)   Ra = 49.999;
  xc = 2500.0 * Xa2 + 50.0 * (Ra-50.0) * (Xa2+Ra2);
  if ((Ra > 50.0 || Xa > 0.0) && xc >= 0.0) {
    xc = ( 50.0 * Xa - sqrt(xc) ) / ( Ra - 50.0 );
    if (xc >= 0.0)  printf ("WARNING, Non-negative number,  Xco = %10.3e\n", xc);
    c = 1.0 / (pif * fabs(xc));

    /* Compute (Co) nearest to, but greater than c */
    if (c > cap2_max) {
      printf ("WARNING, Maximum capacitance of %s exceeded.", num_str(cap2_max,10,string));
      printf ("  --> Co = %10.3e\n", c);
      *Co = cap2_max;
    }
    else {
      /* Note:  The function "ceil()" returns the nearest rounded-up integer */
      *Co = ceil(c/cap_inc) * cap_inc;
    }

    /* Compute new Ra and Xa from old values of Ra,Xa and computed xc */
    xc = -1.0 / (pif * (*Co));
    xcxa = xc+Xa;
    Ra = (Ra * xc*xc) / (Ra2 + xcxa*xcxa);
    Xa = (xc * (Ra2 + Xa * xcxa)) / (Ra2 + xcxa*xcxa);
    if (Xa >= 0.0)  printf ("WARNING, Non-negative number,  Xa = %10.3e\n", Xa);
  }
  else
    *Co = 0.0;
```

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```
  for (i=0; i<2; i++) {
    /* Compute Ci and L */
    if (Ra >= 50.0)   Ra = 49.99999;    /* Equations fail if Ra >= 50, fudge it */
    xc = -50.0 * sqrt( Ra/(50.0-Ra) );
    if (xc >= 0.0)  printf ("WARNING, Non-negative number,  Xci = %10.3e\n", xc);
    *L = ( (-50.0 * Ra)/xc - Xa ) / pif;

    /* Compute (L) nearest actual L */
    if (*L > ind_max) {
      printf ("WARNING, Maximum inductance of %10.3e exceeded.", ind_max);
      printf ("  ==> L = %10.3e\n", *L);
      *L = ind_max;
    }
    else
      *L = (int)(*L/ind_inc+0.5) * ind_inc;

    c = 1.0 / (pif * fabs(xc));
    Ra += (pif * (*L)) / Q;       /* Adjust Ra for Q, then recompute Ci & L */
  }

  /* Compute (Ci) nearest to c */
  if (c > capl_max) {
    printf ("WARNING, Maximum capacitance of %10.3e exceeded.", capl_max);
    printf ("  ==> Ci = %10.3e\n", c);
    *Ci = capl_max;
  }
  else
    *Ci = (int)(c/cap_inc+0.5) * cap_inc;
}
/* ------------------------------------------------------------------------ */
```

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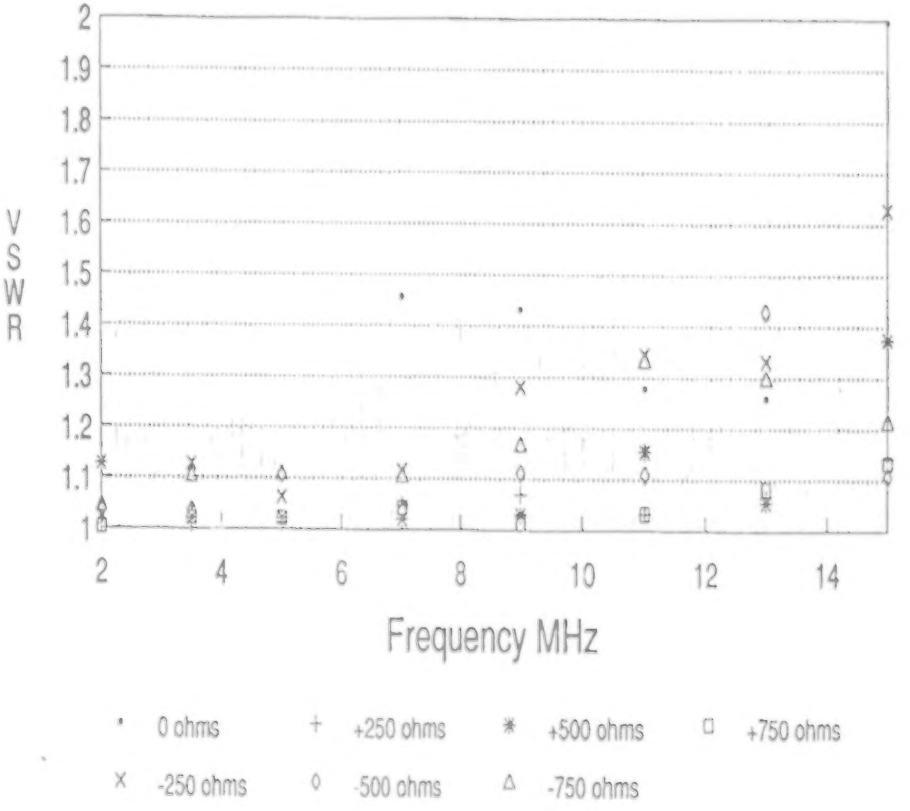
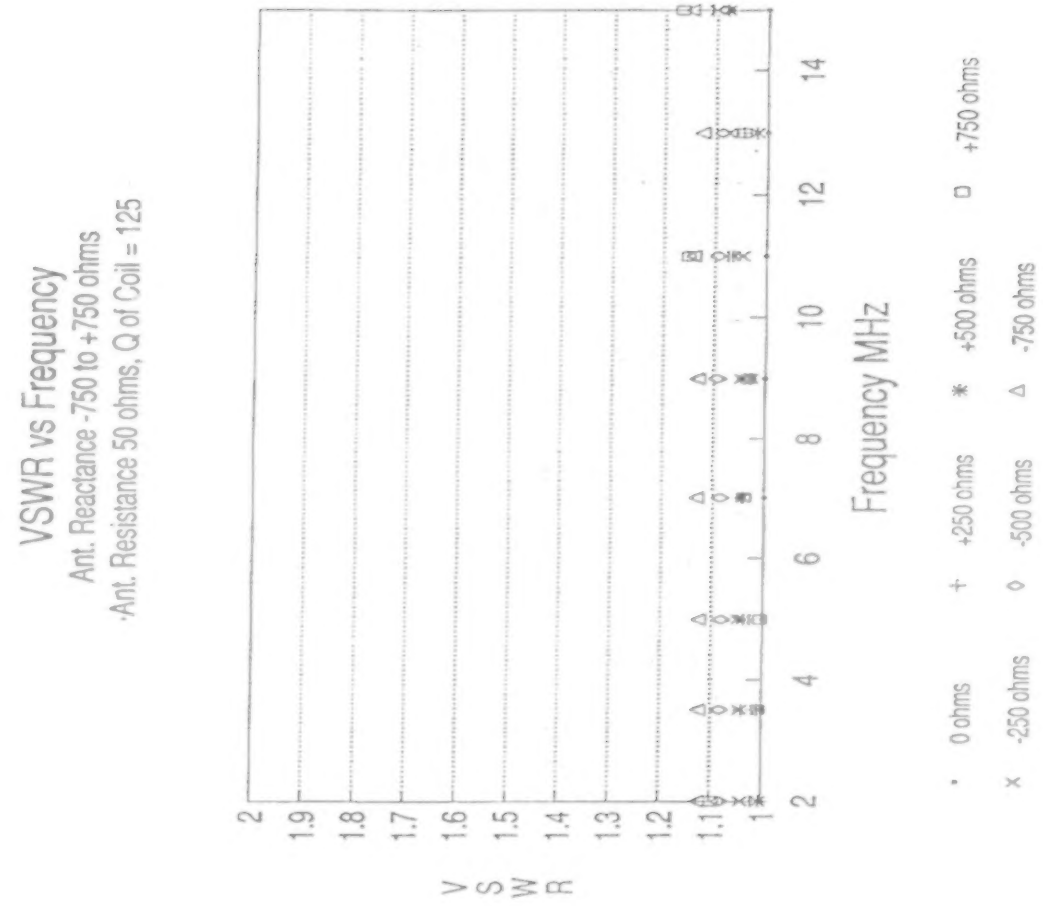
# VSWR with Frequency

Ant. Reactance -750 to +750 ohms

Ant Resistance 5 ohms, Q of Coil = 125




VSWR vs Frequency
Ant. Reactance -750 to +750 ohms
Ant. Resistance 50 ohms, Q of Coil = 125
VSWR
2
1.9
1.8
1.7
1.6
1.5
1.4
1.3
1.2
1.1
1
2
4
6
8
10
12
14
Frequency MHz
0 ohms
+250 ohms
+500 ohms
+750 ohms
-250 ohms
-500 ohms
-750 ohms

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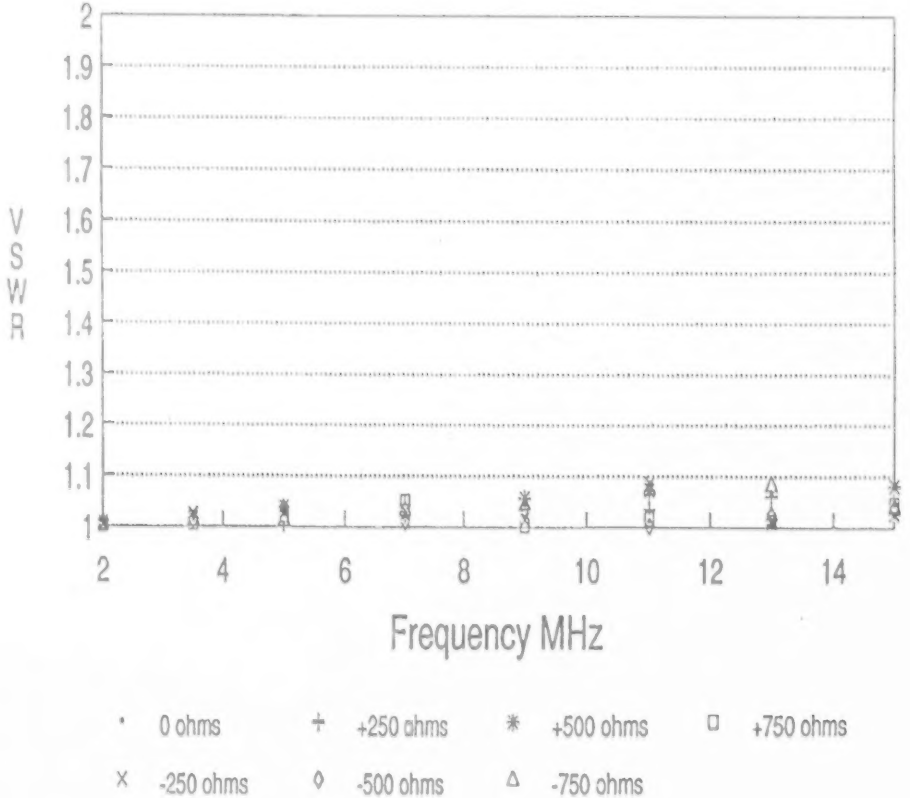
# VSWR with Frequency

Ant. Reactance -750 to +750 ohms

Ant. Resist. 1000 ohms, Q of Coil = 125



# APPENDIX E

## COMPUTATION OF FINAL VALUES OF Ls, Ci, and Co
## LISTING OF COMPUTER PROGRAM

```
/* Define Global Variables */
double target_vswr = 1.6;      /* Target VSWR at which to stop fine tuning */
int    max_count   = 10;       /* Maximum number component changes allowed */
int    count       = 0;        /* Total number of component changes */

/* Define Component Arrays */
double ind_inc  =   0.1e-06;  /* Incremental value of inductance available  */
double cap_inc  =  12.5e-12;  /* Incremental value of capacitance available */
double ind_max  = 200.0e-06;  /* Maximum value of inductance available      */
double cap1_max = 6387.5e-12; /* Maximum value of input capacitance avail.  */
double cap2_max = 4000.0e-12; /* Maximum value of output capacitance avail. */

void tweak ( double *L, double *Ci, double *Co, double *vswr );
int Tweak_cmp ( int cmp_id, float pskip,
                double *L, double *Ci, double *Co, double *vswr );

main()
{
  double L, Ci, Co, vswr;
  L    = 0; /* ?????  * Current inductance */
  Ci   = 0; /* ?????  * Current input capacitance */
  Co   = 0; /* ?????  * Current output capacitance */
  vswr = 0; /* ?????  * Current measurement of vswr */

  tweak (&L, &Ci, &Co, &vswr);   /* fine tune the circuit */
}


/* ============================================================================
TWEAK - Routine used to fine tune the circuit minor variations in the
        values of inductance, input capacitance and output capacitance.

Global Constants:
  Largest_vswr -  Target vswr at which to stop fine tuning.
  ind_inc      -  Incremental values of inductance available.
  ind_max      -  Maximum value of inductance available.
  cap_inc      -  Incremental values of capacitance available.
  cap1_max     -  Maximum value of input capacitance available.
  cap2_max     -  Maximum value of output capacitance available.

Input:
  vswr -  Current measured value of VSWR.
  L    -  Current value of inductance.
  Ci   -  Current value for input capacitance.
  Co   -  Current value for output capacitance.

Output:
  vswr -  Adjusted measured value of VSWR.
  L    -  Adjusted value of inductance.
  Ci   -  Adjusted value for input capacitance.
  Co   -  Adjusted value for output capacitance.
============================================================================ */

void tweak ( double *L, double *Ci, double *Co, double *vswr )
{
  int i, cid;
  double pskip, last_vswr;

  count = 0;                  /* Initialize number of VSWR measurements to zero */
  pskip = 0.05;               /* Set initial stepping increment to 5% */
  for (i=0; *vswr > target_vswr && last_vswr-(*vswr) > 1.0e-6 && count < max_count; cid++) {
    last_vswr = *vswr;
    for (cid=0; cid<3 && *vswr > target_vswr && count < max_count; cid++) {
      pskip = log(*vswr/0.995) * 0.14;
      pskip = (pskip > 0.2) ? 0.2 : pskip;
      count += Tweak_cmp (cid, pskip, L, Ci, Co, vswr);
    }
  }
}
```

```
#define  OUT_CAPACITOR  0      /* Defines the component tweaking order */
#define  INDUCTOR       1
#define  IN_CAPACITOR   2

int Tweak_cmp ( int cmp_id, float pskip,
                double *L, double *Ci, double *Co, double *vswr )
{
  int    cnt, offset_cntrl;
  double pivot, old_pivot, test_vswr, offset, sm_offset;
  double *cmp;

  switch (cmp_id) {
    case INDUCTOR:     cmp = L;   sm_offset = ind_inc;   break;
    case IN_CAPACITOR: cmp = Ci;  sm_offset = cap_inc;   break;
    case OUT_CAPACITOR: cmp = Co; sm_offset = cap_inc;   break;
  }
  /* NOTE:  cmp is a pointer to either L, Ci or Co.  If the value of cmp
            is changed, its pointed to value of L, Ci, Co is also changed. */

  cnt = 0;
  pivot = *cmp;
  old_pivot = pivot;

  /* Compute initial offset rounded to nearest component increment */
  offset = (int)((pivot*pskip)/sm_offset+0.5) * sm_offset;
  if (offset <= sm_offset)
    offset = sm_offset;

  offset_cntrl = 1;
  while (pivot==old_pivot && fabs(offset) >= sm_offset && count+cnt < max_count) {
    *cmp = pivot + offset;          /* compute next test point (+/-)offset */
    if (*cmp < 0.0)  *cmp = 0.0;    /* component values can not be negative */

    Set_Switches (*L, *Ci, *Co);    /* set component switches */
    test_vswr = Measure_vswr();     /* measure vswr */
    ++cnt;                          /* count number of component changes */

    if (test_vswr < *vswr) {        /* Has VSWR improved ? */
      pivot = *cmp;                 /* if yes: New pivot point */
      *vswr = test_vswr;
    }
    else if (cnt==1 && pivot!=0.0) /* if no:  Reverse direction or   */
      offset *= -1;                /*         reduce offset by one quarter */
    else
      offset_cntrl = ( (offset_cntrl==4 && pivot != 0.0) ? -1 : 4 );
    offset /= offset_cntrl;
  }
  *cmp = pivot;
  return (cnt);
}
```

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# APPENDIX F

## LISTING OF TEST, READ AND DISPLAY PROGRAMS

EXAMPLES.ASM

```
; Example code on programming the fiber optics interface
; This code will execute once, and then return to DOS
; It is recommended that I/O to the fiber optics interface be
; imbedded in the main controller code, as this is the fastest method
; Calling subroutines requires extra CPU time
; This code can be converted into "C" calls, although slower
; Or this assembler code can be imbedded in the C code
;
;
;
CODE   SEGMENT BYTE PUBLIC 'CODE'
       ASSUME CS:CODE,DS:DATA
;
;
; Declare I/O addresses
;
OUTLO     EQU 0300h          ; Low word for PIN diodes
OUTHI     EQU 0302h          ; High word, all 32 bits transferred
STRB      EQU 0304h          ; Request data from A/Ds
CLRRDY    EQU 0306h          ; Clear data ready flag, to accept more data
;
AD0       EQU 0300h          ; A/D Channel 0   (fwd voltage), 12 LSBs
AD1       EQU 0302h          ; A/D Channel 1   (rev voltage), 12 LSBs
AD2       EQU 0304h          ; A/D Channel 2   (phase), 12 LSBs
AD3       EQU 0306h          ; A/D Channel 3   (phase ref), 12 LSBs
QUAD      EQU 0308h          ; Phase Quadrant bit (B15)
NS        EQU 030Ah          ; Frequency count, 12 LSBs
NC        EQU 030Ch          ; Number of cycles, 12 LSBs
DATRDY    EQU 030Eh          ; Data ready flag (B15)
;
;
START:
;
; Program pattern for PIN diode drivers
; Example 32-bit word here is 12345678 hex
;
          MOV DX,OUTLO       ; Load DX with I/O address of LO order latch
          MOV AX,5678h       ; Load AX with LO order word of pattern
          OUT DX,AX          ; Output to LO order latch
          MOV DX,OUTHI       ; Load DX with I/O address of HI order latch
          MOV AX,1234h       ; Load AX with HI order word of pattern
          OUT DX,AX          ; Output to HI order latch, plus LO word to
                             ; second level latch
;
;
;
;
; The follow code requests and reads data from the A/D interface box
; The fastest possible method is to first issue a RQST pulse,
; then clear the data ready flag (from the previous read)
; However, the flag must be cleared before the data arrives
; To ensure this, interrupts are disabled, avoiding the possibility
; of an interrupt occuring between the STRB pulse and clearing ready flag
; The main background interrupt is a 55 mSec tick from the DOS clock
; Service time is about 22 uSec
;
;
          CLI                ; Mask-out interrupts for critical code
;
```

```
; Trigger RQST mono, to request data from A/D interface box
;
        MOV DX,STRB         ; Load DX with I/O address of RQST trigger
        OUT DX,AX           ; Output to address generates RQST pulse
                            ; Data in AX is don't care
;
;
; Clear ready flag
;
        MOV DX,CLRRDY       ; Load DX with I/O address of clear pulse
        OUT DX,AX           ; Output to address generates clear pulse
                            ; Data in AX is don't care
;
;
        STI                 ; Re-enable interrupts, critical code complete
;
;
        MOV BX,0            ; Load time-out count
        MOV DX,DATRDY       ; Load DX with I/O address of ready flag
;
; Wait until ready flag goes high
; but don't wait forever if no response from A/D interface
;
DATWT:  IN AX,DX            ; Get data ready flag into AX (MSB is flag bit)
        DEC BX              ; Decrement time-out counter
        JZ TIMEOUT          ; If decremented to zero, jump to time-out handler
        AND AX,8000h        ; Test MSB of AX (ready flag)
        JZ DATWT            ; Loop back if low (no data available yet)
;
;
; Read data
;
        MOV DX,AD0          ; Load address of A/D channel 0 into DX
        IN AX,DX            ; Read A/D channel 0 data into AX
;
        MOV DX,AD1          ; Load address of A/D channel 1 into DX
        IN AX,DX            ; Read A/D channel 1 data into AX
;
        MOV DX,AD2          ; Load address of A/D channel 2 into DX
        IN AX,DX            ; Read A/D channel 2 data into AX
;
        MOV DX,AD3          ; Load address of A/D channel 3 into DX
        IN AX,DX            ; Read A/D channel 3 data into AX
;
        MOV DX,QUAD         ; Load address of phase quadrant into DX
        IN AX,DX            ; Read phase quadrant register into AX
        AND AX,8000h        ; Mask-out non-valid data
;
        MOV DX,NS           ; Load address of NS (frequency) into DX
        IN AX,DX            ; Read NS data into AX
;
        MOV DX,NC           ; Load address of NC (frequency) into DX
        IN AX,DX            ; Read NC data into AX
;
;
; End of I/O code, return to DOS since example is finished
;
;
TIMEOUT:                    ; Time-out also returns to DOS
                            ; a proper time-out handler can be put here
;
        MOV AH,4Ch          ; Return to DOS
        MOV AL,00h          ; using standard BIOS call
        INT 21h
```

```
;
CODE   ENDS                ; End of code segment
;
;
DATA   SEGMENT WORD PUBLIC 'DATA'
DATA   ENDS
;
STACK  SEGMENT WORD STACK 'STACK'
STACK  ENDS
;
       END START           ; Starting address is START
```

```
; Full test program
; Provides 32-bit rotating bit pattern on PIN drivers
; Reads and displays data
;
CODE   SEGMENT BYTE PUBLIC 'CODE'
       ASSUME CS:CODE,DS:DATA
;
OUTLO    EQU 0300h          ; Low word for PIN diodes
OUTHI    EQU 0302h          ; High word, all 32 bits transferred
STRB     EQU 0304h          ; Request data from A/Ds
CLRRDY   EQU 0306h          ; Clear data ready flag, to accept more data
;
AD0      EQU 0300h          ; A/D Channel 0  (fwd voltage), 12 LSBs
AD1      EQU 0302h          ; A/D Channel 1  (rev voltage), 12 LSBs
AD2      EQU 0304h          ; A/D Channel 2  (phase), 12 LSBs
AD3      EQU 0306h          ; A/D Channel 3  (phase ref), 12 LSBs
QUAD     EQU 0308h          ; Phase Quadrant bit (B15)
NS       EQU 030Ah          ; Frequency count, 12 LSBs
NC       EQU 030Ch          ; Number of cycles, 12 LSBs
DATRDY   EQU 030Eh          ; Data ready flag (B15)
;
;
START:
;
         PUSH DS            ; Save DS
         MOV AX,CS          ; Set DS = CS
         MOV DS,AX
;
AGAIN:
;
         MOV DX,OUTLO       ; Set all LEDs on
         MOV AX,0FFFFh
         OUT DX,AX
         MOV DX,OUTHI
         MOV AX,0FFFFh
         OUT DX,AX
;
         MOV DX,OUTLO       ; Set all 32 bits to zeros
         MOV AX,0000h
         OUT DX,AX
         MOV DX,OUTHI
         MOV AX,0000h
         OUT DX,AX
;
         MOV DX,OUTLO       ; Rotate PIN control bit around 32 locations
         MOV AX,0001h
         OUT DX,AX
         MOV DX,OUTHI       ; Load HI word and transfer to Driver Box
         MOV AX,0000h
         OUT DX,AX
;
         MOV DX,OUTLO
         MOV AX,0002h
         OUT DX,AX
         MOV DX,OUTHI
         MOV AX,0000h
         OUT DX,AX
;
         MOV DX,OUTLO
         MOV AX,0004h
         OUT DX,AX
         MOV DX,OUTHI
         MOV AX,0000h
         OUT DX,AX
```

```
;
        MOV DX,OUTLO
        MOV AX,0008h
        OUT DX,AX
        MOV DX,OUTHI
        MOV AX,0000h
        OUT DX,AX
;
        MOV DX,OUTLO
        MOV AX,0010h
        OUT DX,AX
        MOV DX,OUTHI
        MOV AX,0000h
        OUT DX,AX
;
        MOV DX,OUTLO
        MOV AX,0020h
        OUT DX,AX
        MOV DX,OUTHI
        MOV AX,0000h
        OUT DX,AX
;
        MOV DX,OUTLO
        MOV AX,0040h
        OUT DX,AX
        MOV DX,OUTHI
        MOV AX,0000h
        OUT DX,AX
;
        MOV DX,OUTLO
        MOV AX,0080h
        OUT DX,AX
        MOV DX,OUTHI
        MOV AX,0000h
        OUT DX,AX
;
        MOV DX,OUTLO
        MOV AX,0100h
        OUT DX,AX
        MOV DX,OUTHI
        MOV AX,0000h
        OUT DX,AX
;
        MOV DX,OUTLO
        MOV AX,0200h
        OUT DX,AX
        MOV DX,OUTHI
        MOV AX,0000h
        OUT DX,AX
;
        MOV DX,OUTLO
        MOV AX,0400h
        OUT DX,AX
        MOV DX,OUTHI
        MOV AX,0000h
        OUT DX,AX
;
        MOV DX,OUTLO
        MOV AX,0800h
        OUT DX,AX
        MOV DX,OUTHI
        MOV AX,0000h
        OUT DX,AX
;
```

```
        MOV DX,OUTLO
        MOV AX,1000h
        OUT DX,AX
        MOV DX,OUTHI
        MOV AX,0000h
        OUT DX,AX
;
        MOV DX,OUTLO
        MOV AX,2000h
        OUT DX,AX
        MOV DX,OUTHI
        MOV AX,0000h
        OUT DX,AX
;
        MOV DX,OUTLO
        MOV AX,4000h
        OUT DX,AX
        MOV DX,OUTHI
        MOV AX,0000h
        OUT DX,AX
;
        MOV DX,OUTLO
        MOV AX,8000h
        OUT DX,AX
        MOV DX,OUTHI
        MOV AX,0000h
        OUT DX,AX
;
;
        MOV DX,OUTLO
        MOV AX,0000h
        OUT DX,AX
        MOV DX,OUTHI
        MOV AX,0001h
        OUT DX,AX
;
        MOV DX,OUTLO
        MOV AX,0000h
        OUT DX,AX
        MOV DX,OUTHI
        MOV AX,0002h
        OUT DX,AX
;
        MOV DX,OUTLO
        MOV AX,0000h
        OUT DX,AX
        MOV DX,OUTHI
        MOV AX,0004h
        OUT DX,AX
;
        MOV DX,OUTLO
        MOV AX,0000h
        OUT DX,AX
        MOV DX,OUTHI
        MOV AX,0008h
        OUT DX,AX
;
        MOV DX,OUTLO
        MOV AX,0000h
        OUT DX,AX
        MOV DX,OUTHI
        MOV AX,0010h
        OUT DX,AX
;
```

```
        MOV DX,OUTLO
        MOV AX,0000h
        OUT DX,AX
        MOV DX,OUTHI
        MOV AX,0020h
        OUT DX,AX
;
        MOV DX,OUTLO
        MOV AX,0000h
        OUT DX,AX
        MOV DX,OUTHI
        MOV AX,0040h
        OUT DX,AX
;
        MOV DX,OUTLO
        MOV AX,0000h
        OUT DX,AX
        MOV DX,OUTHI
        MOV AX,0080h
        OUT DX,AX
;
        MOV DX,OUTLO
        MOV AX,0000h
        OUT DX,AX
        MOV DX,OUTHI
        MOV AX,0100h
        OUT DX,AX
;
        MOV DX,OUTLO
        MOV AX,0000h
        OUT DX,AX
        MOV DX,OUTHI
        MOV AX,0200h
        OUT DX,AX
;
        MOV DX,OUTLO
        MOV AX,0000h
        OUT DX,AX
        MOV DX,OUTHI
        MOV AX,0400h
        OUT DX,AX
;
        MOV DX,OUTLO
        MOV AX,0000h
        OUT DX,AX
        MOV DX,OUTHI
        MOV AX,0800h
        OUT DX,AX
;
        MOV DX,OUTLO
        MOV AX,0000h
        OUT DX,AX
        MOV DX,OUTHI
        MOV AX,1000h
        OUT DX,AX
;
        MOV DX,OUTLO
        MOV AX,0000h
        OUT DX,AX
        MOV DX,OUTHI
        MOV AX,2000h
        OUT DX,AX
;
        MOV DX,OUTLO
```

```
          MOV AX,0000h
          OUT DX,AX
          MOV DX,OUTHI
          MOV AX,4000h
          OUT DX,AX
;
          MOV DX,OUTLO
          MOV AX,0000h
          OUT DX,AX
          MOV DX,OUTHI
          MOV AX,8000h
          OUT DX,AX
;
;
          MOV DX,OUTLO      ; Set all 32 bits to zeros
          MOV AX,0000h
          OUT DX,AX
          MOV DX,OUTHI
          MOV AX,0000h
          OUT DX,AX
;
;
          CLI               ; Mask-out interrupts
;
          MOV DX,STRB       ; Pulse 10 uSec mono (RQST)
          OUT DX,AX
;
          MOV DX,CLRRDY     ; Clear ready flag
          OUT DX,AX
;
          STI               ; Re-enable interrupts
;
          MOV BX,0          ; Load time-out count
          MOV DX,DATRDY
DATWT:    IN AX,DX          ; Get data ready flag
          DEC BX            ; Time-out check
          JZ TIMEOUT
          AND AX,8000h      ; Test MSB
          JZ DATWT          ; Loop back if low
;
;
;
; Format for display of data is:
;
;AD0=abcd  AD1=abcd  AD2=abcd  AD3=abcd  QUAD=abcd  NS=abcd  NC=abcd
;
          MOV DI,OFFSET MESS1
          CALL DISPMESS
          MOV DX,AD0        ; Read and display A/D channel 0
          IN AX,DX
          CALL DISPHEX
;
          MOV DI,OFFSET MESS2
          CALL DISPMESS
          MOV DX,AD1        ; Read and display A/D channel 1
          IN AX,DX
          CALL DISPHEX
;
          MOV DI,OFFSET MESS3
          CALL DISPMESS
          MOV DX,AD2        ; Read and display A/D channel 2
          IN AX,DX
          CALL DISPHEX
;
```

```
        MOV DI,OFFSET MESS4
        CALL DISPMESS
        MOV DX,AD3          ; Read and display A/D channel 3
        IN AX,DX
        CALL DISPHEX
;
        MOV DI,OFFSET MESS5
        CALL DISPMESS
        MOV DX,QUAD         ; Read and display phase quadrant
        IN AX,DX
        AND AX,0FF00h       ; Mask-out 8 LSBs
        CALL DISPHEX
;
        MOV DI,OFFSET MESS6
        CALL DISPMESS
        MOV DX,NS           ; Read and display NS
        IN AX,DX
        CALL DISPHEX
;
        MOV DI,OFFSET MESS7
        CALL DISPMESS
        MOV DX,NC           ; Read and display NC
        IN AX,DX
        CALL DISPHEX
;
        MOV DI,OFFSET CRLF
        CALL DISPMESS
;
        MOV AH,06
        MOV DL,0FFh         ; request input from keyboard
        INT 21h
        JNZ CHKESC          ; jump if character available
        JMP AGAIN
CHKESC: CMP AL,1Bh          ; check for Esc
        JE DONE
        JMP AGAIN
        JMP AGAIN
;
TIMEOUT:
        MOV DI,OFFSET MESS8
        CALL DISPMESS
;
DONE:
        POP DS              ; Restore DS
;
        MOV AH,4Ch          ; Return to DOS
        MOV AL,00h
        INT 21h
;
;
;
DISPMESS  PROC NEAR
; Display string via DI
GETCH:  MOV DL,[DI]         ; Get char
        CMP DL,0            ; If NUL, exit
        JZ ENDSTR
        MOV AH,2
        INT 21h
        INC DI
        JMP GETCH
;
ENDSTR: RET
DISPMESS  ENDP
;
```

```
;
DISPHEX   PROC NEAR
; Convert 16-bit unsigned integer in AX to hexadecimal to display value
;
          MOV BX,AX
          MOV AH,2          ; Select display function
          MOV DL,BH
          SHR DL,1
          SHR DL,1
          SHR DL,1
          SHR DL,1
          ADD DL,'0'
          CMP DL,'9'
          JLE TYPE1
          ADD DL,'A'-'0'-10
TYPE1:    INT 21h
;
          MOV DL,BH
          AND DL,0Fh
          ADD DL,'0'
          CMP DL,'9'
          JLE TYPE2
          ADD DL,'A'-'0'-10
TYPE2:    INT 21h
;
          MOV DL,BL
          SHR DL,1
          SHR DL,1
          SHR DL,1
          SHR DL,1
          ADD DL,'0'
          CMP DL,'9'
          JLE TYPE3
          ADD DL,'A'-'0'-10
TYPE3:    INT 21h
;
          MOV DL,BL
          AND DL,0Fh
          ADD DL,'0'
          CMP DL,'9'
          JLE TYPE4
          ADD DL,'A'-'0'-10
TYPE4:    INT 21h
          RET
DISPHEX   ENDP
;
;
MESS1     DB 'AD0='
          DB 0              ; End of message
MESS2     DB '  AD1='
          DB 0
MESS3     DB '  AD2='
          DB 0
MESS4     DB '  AD3='
          DB 0
MESS5     DB '  QUAD='
          DB 0
MESS6     DB '  NS='
          DB 0
MESS7     DB '  NC='
          DB 0
CRLF      DB 0Dh
          DB 0Ah
          DB 0
```

```
MESS8    DB 'Time-out on data ready flag'
         DB ODh
         DB OAh
         DB 0
;
;
CODE  ENDS
;
;
DATA  SEGMENT WORD PUBLIC 'DATA'
DATA  ENDS
;
STACK SEGMENT WORD STACK 'STACK'
STACK ENDS
;
      END START
```

SETPINS.ASM

```
; Test Petrie PIN diode interface
; Input 32-bit hex long word from keyboard, and set the outputs
;
;
STACK SEGMENT WORD STACK 'STACK'
STACK ENDS
;
DATA   SEGMENT WORD PUBLIC 'DATA'
DATA   ENDS
;
CODE   SEGMENT BYTE PUBLIC 'CODE'
       ASSUME CS:CODE,DS:DATA
;
OUTLO    EQU 0300h
OUTHI    EQU 0302h
STRB     EQU 0304h
;
START:
         PUSH DS           ; Save DS
         MOV AX,CS         ; Set DS = CS
         MOV DS,AX
;
NEWVAL:  MOV DI,OFFSET PROMPT
         CALL DISPMESS
;
; Init pointers
         MOV DI,OFFSET CHARBUF
         MOV BX,0
;
GETCHAR:
         MOV AH,01h
         INT 21h           ; Wait for keyboard
         CMP AL,08         ; Check for backspace
         JNE CHKCHR
         CMP BX,0          ; Check buffer pointer
         JZ GETCHAR
         DEC BX            ; back-up pointers
         DEC DI
         JMP GETCHAR
CHKCHR:  AND AL,7Fh        ; strip MSB
         CMP AL,'f'        ; check for out of range characters
         JLE NXT1
         JMP ERR
NXT1:    CMP AL,'a'
         JL UCASE
         SUB AL,'a'-'A'    ; convert to upper case hex
UCASE:   CMP AL,'F'
         JLE NXT2
         JMP ERR
NXT2:    CMP AL,'A'
         JGE NXT3
         CMP AL,'9'
         JLE NXT3
         JMP ERR
NXT3:    CMP AL,'0'
         JGE NXT4
         CMP AL,0Dh
         JE NXT4
         CMP AL,1Bh        ; check for Esc char
         JE EXIT1
```

```
        JMP ERR
;
EXIT1:  JMP EXIT
;
NXT4:   MOV [DI],AL         ; store in buffer
        CMP AL,0Dh          ; check for Enter char
        JE ENTER
;
        CMP BX,100          ; check buffer pointer limit
        JE GETCHAR          ; don't inc if at limit
        INC BX              ; if not, inc pointers
        INC DI
        JMP GETCHAR
;
ENTER:  CMP BX,0            ; if nothing in buffer, exit
        JNZ INITZ
        JMP ERR
;
INITZ:  DEC BX              ; back-up pointers to just before Enter
        DEC DI
        MOV DX,0            ; assume leading zeros
        MOV CX,0
;
        MOV AL,[DI]         ; last hex get char
        SUB AL,'0'          ; convert hex to binary
        CMP AL,9
        JLE OVER1
        ADD AL,'0'
        SUB AL,'A'-10
OVER1:  MOV DL,AL
        CMP BX,0            ; Check if any more data
        JNE DEC1
        JMP OUTLEDS
;
DEC1:   DEC BX
        DEC DI
        MOV AL,[DI]         ; last hex get char
        SUB AL,'0'          ; convert hex to binary
        CMP AL,9
        JLE OVER2
        ADD AL,'0'
        SUB AL,'A'-10
OVER2:  SHL AL,1
        SHL AL,1
        SHL AL,1
        SHL AL,1
        OR DL,AL
        CMP BX,0            ; Check if any more data
        JNE DEC2
        JMP OUTLEDS
;
DEC2:   DEC BX
        DEC DI
        MOV AL,[DI]         ; last hex get char
        SUB AL,'0'          ; convert hex to binary
        CMP AL,9
        JLE OVER3
        ADD AL,'0'
        SUB AL,'A'-10
OVER3:  MOV DH,AL
        CMP BX,0            ; Check if any more data
        JNE DEC3
        JMP OUTLEDS
;
```

```
DEC3:   DEC BX
        DEC DI
        MOV AL,[DI]      ; last hex get char
        SUB AL,'0'       ; convert hex to binary
        CMP AL,9
        JLE OVER4
        ADD AL,'0'
        SUB AL,'A'-10
OVER4:  SHL AL,1
        SHL AL,1
        SHL AL,1
        SHL AL,1
        OR DH,AL
        CMP BX,0         ; Check if any more data
        JNE DEC4
        JMP OUTLEDS
;
; Convert HI word (if non-zero) to binary
DEC4:   DEC BX
        DEC DI
        MOV AL,[DI]      ; last hex get char
        SUB AL,'0'       ; convert hex to binary
        CMP AL,9
        JLE OVER5
        ADD AL,'0'
        SUB AL,'A'-10
OVER5:  MOV CL,AL
        CMP BX,0         ; Check if any more data
        JNE DEC5
        JMP OUTLEDS
;
DEC5:   DEC BX
        DEC DI
        MOV AL,[DI]      ; last hex get char
        SUB AL,'0'       ; convert hex to binary
        CMP AL,9
        JLE OVER6
        ADD AL,'0'
        SUB AL,'A'-10
OVER6:  SHL AL,1
        SHL AL,1
        SHL AL,1
        SHL AL,1
        OR CL,AL
        CMP BX,0         ; Check if any more data
        JNE DEC6
        JMP OUTLEDS
;
DEC6:   DEC BX
        DEC DI
        MOV AL,[DI]      ; last hex get char
        SUB AL,'0'       ; convert hex to binary
        CMP AL,9
        JLE OVER7
        ADD AL,'0'
        SUB AL,'A'-10
OVER7:  MOV CH,AL
        CMP BX,0         ; Check if any more data
        JNE DEC7
        JMP OUTLEDS
;
DEC7:   DEC BX
        DEC DI
        MOV AL,[DI]      ; last hex get char
```

```
        SUB AL,'0'          ; convert hex to binary
        CMP AL,9
        JLE OVER8
        ADD AL,'0'
        SUB AL,'A'-10
OVER8:  SHL AL,1
        SHL AL,1
        SHL AL,1
        SHL AL,1
        OR CH,AL
;
OUTLEDS:
        MOV DI,OFFSET CRLF
        CALL DISPMESS
        MOV DI,OFFSET MESS1
        CALL DISPMESS
        MOV AX,CX
        CALL DISPHEX
        MOV DI,OFFSET MESS2
        CALL DISPMESS
        MOV AX,DX
        CALL DISPHEX
        MOV DI,OFFSET CRLF
        CALL DISPMESS
;
        MOV AX,DX
        MOV DX,OUTLO
        OUT DX,AX
        MOV AX,CX
        MOV DX,OUTHI
        OUT DX,AX
;
        JMP NEWVAL
;
;
ERR:    MOV DI,OFFSET ERRMESS
        CALL DISPMESS
        JMP NEWVAL
;
EXIT:
        POP DS              ; Restore DS
;
        MOV AH,4Ch
        MOV AL,0
        INT 21h             ; Exit to DOS
;
;
DISPMESS  PROC NEAR
; Display string via DI
        PUSH DX
GETCH:  MOV DL,[DI]         ; Get char
        CMP DL,0            ; If NUL, exit
        JZ ENDSTR
        MOV AH,2
        INT 21h
        INC DI
        JMP GETCH
;
ENDSTR: POP DX
        RET
DISPMESS  ENDP
;
;
DISPHEX   PROC NEAR
```

```
; Convert 16-bit unsigned integer in AX to hexadecimal to display value
;
        PUSH DX
        MOV BX,AX
        MOV AH,2            ; Select display function
        MOV DL,BH
        SHR DL,1
        SHR DL,1
        SHR DL,1
        SHR DL,1
        ADD DL,'0'
        CMP DL,'9'
        JLE TYPE1
        ADD DL,'A'-'0'-10
TYPE1:  INT 21h
;
        MOV DL,BH
        AND DL,0Fh
        ADD DL,'0'
        CMP DL,'9'
        JLE TYPE2
        ADD DL,'A'-'0'-10
TYPE2:  INT 21h
;
        MOV DL,BL
        SHR DL,1
        SHR DL,1
        SHR DL,1
        SHR DL,1
        ADD DL,'0'
        CMP DL,'9'
        JLE TYPE3
        ADD DL,'A'-'0'-10
TYPE3:  INT 21h
;
        MOV DL,BL
        AND DL,0Fh
        ADD DL,'0'
        CMP DL,'9'
        JLE TYPE4
        ADD DL,'A'-'0'-10
TYPE4:  INT 21h
        POP DX
        RET
DISPHEX  ENDP
;
;
MESS1   DB 'HI='
        DB 0                ; End of message
MESS2   DB '  LO='
        DB 0
CRLF    DB 0Dh
        DB 0Ah
        DB 0
PROMPT  DB 'Enter 32-bit word for PIN diodes (in hex)'
        DB ', Esc to exit : '
        DB 0
ERRMESS DB 0Dh
        DB 0Ah
        DB '*** Illegal character, nothing written'
        DB 0Dh
        DB 0Ah
```

```
;
CHARBUF   DB 100 DUP (0)
;
CODE   ENDS
;
       END START
```

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